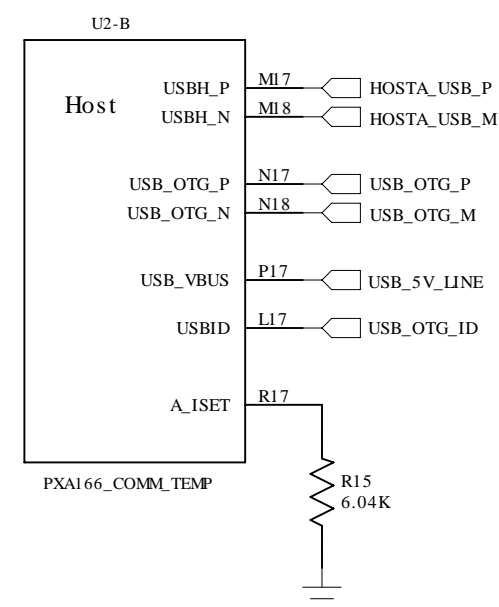


# PXA166 800 MHz - PXA168 1066 MHz

## USB Ports

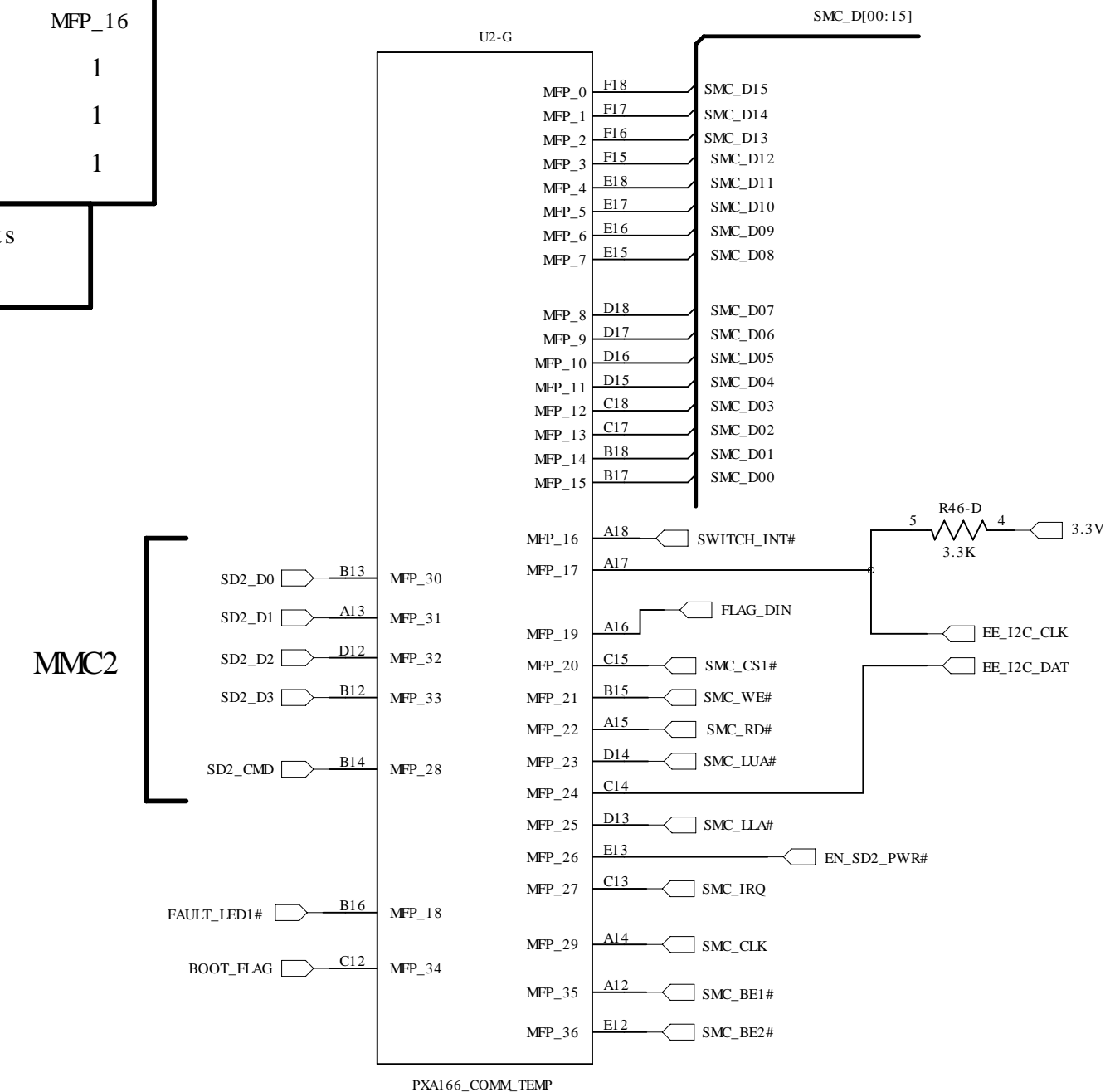


## Board ID

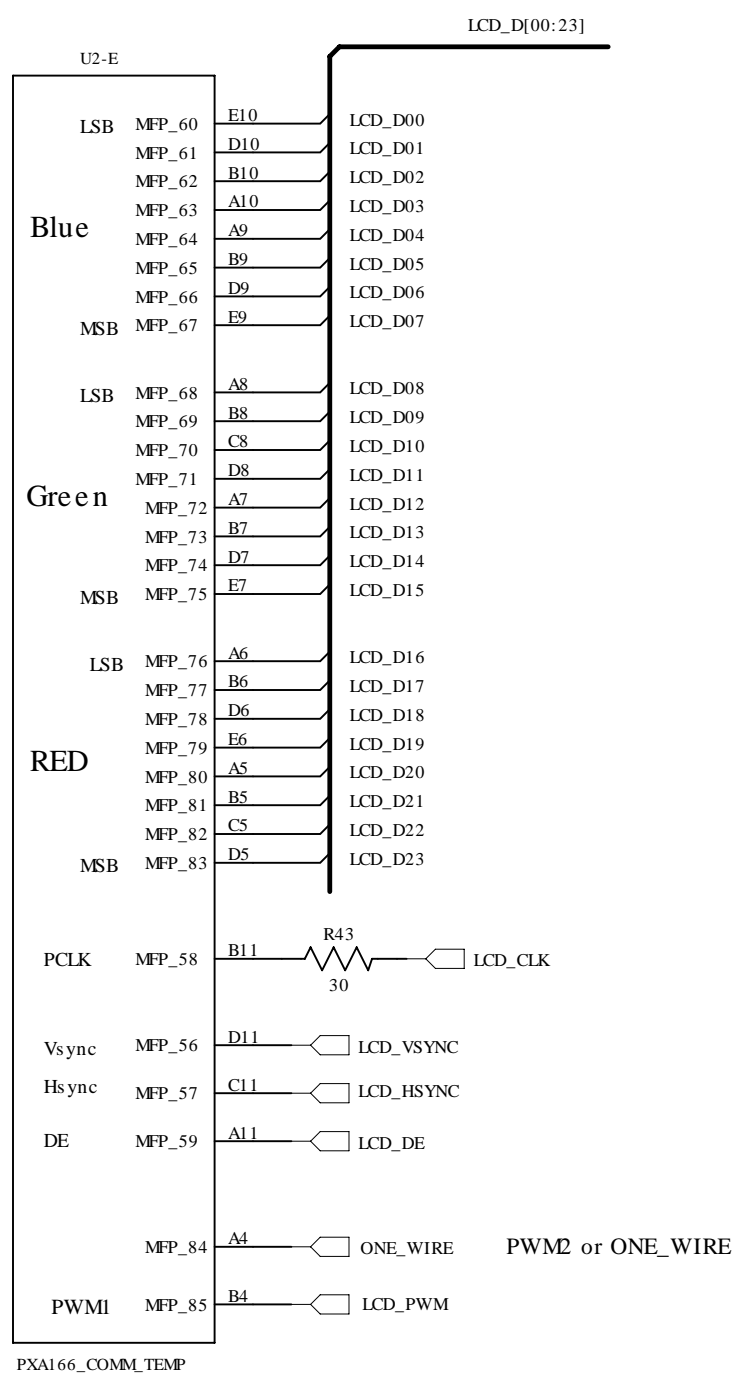
	MFP_19	MFP_17	MFP_16
TS-4710	1	0	1
TS-4712	1	1	1
TS-4720	0	1	1

Requires MFP to be Inputs  
and weak PU turned ON

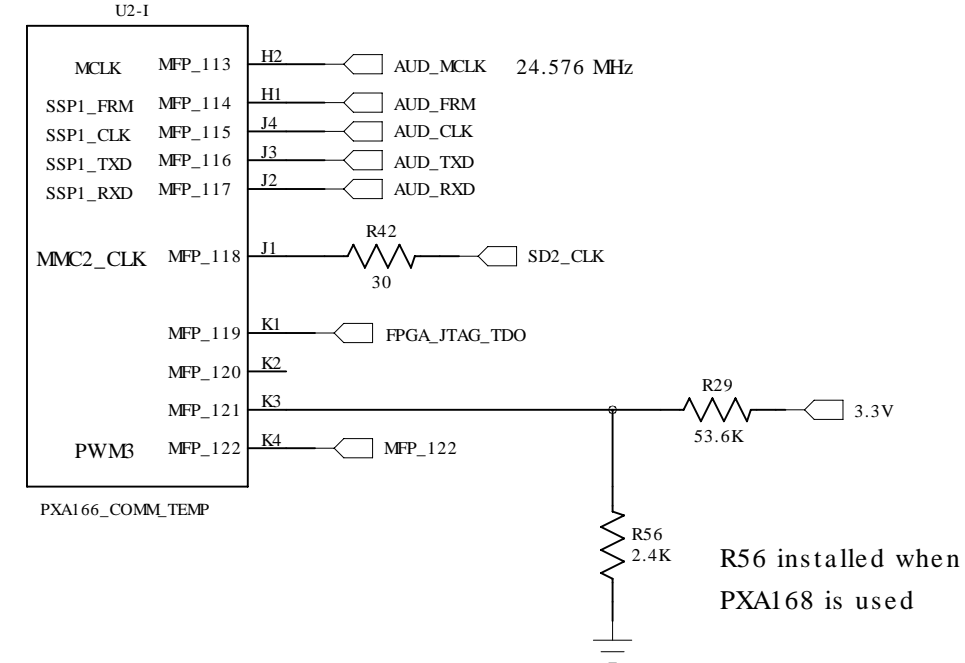
## SMC Bus



## LCD

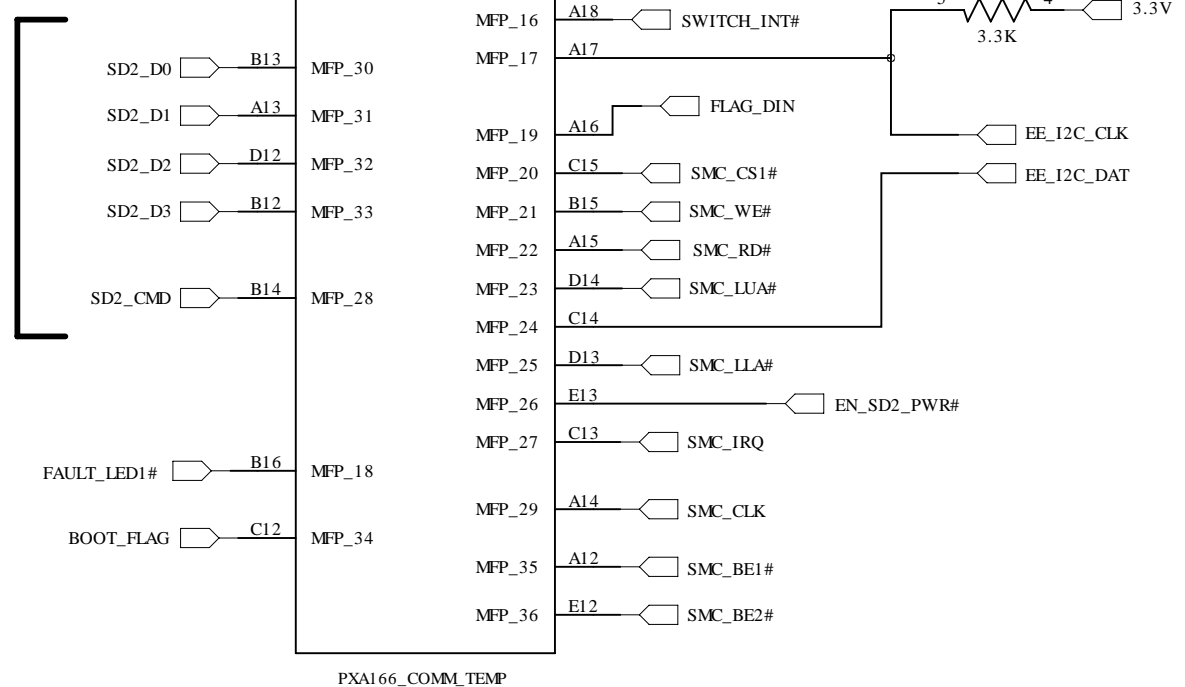


## I2S

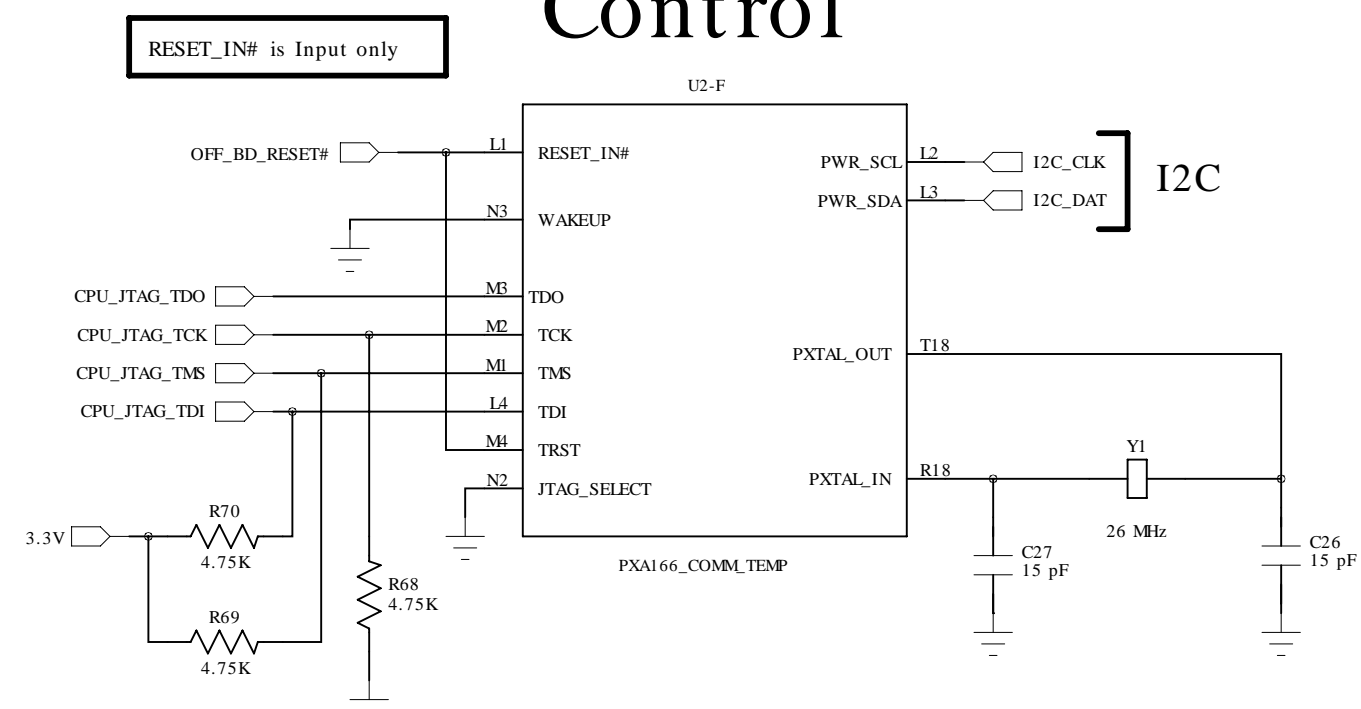


R56 installed when  
PXA168 is used

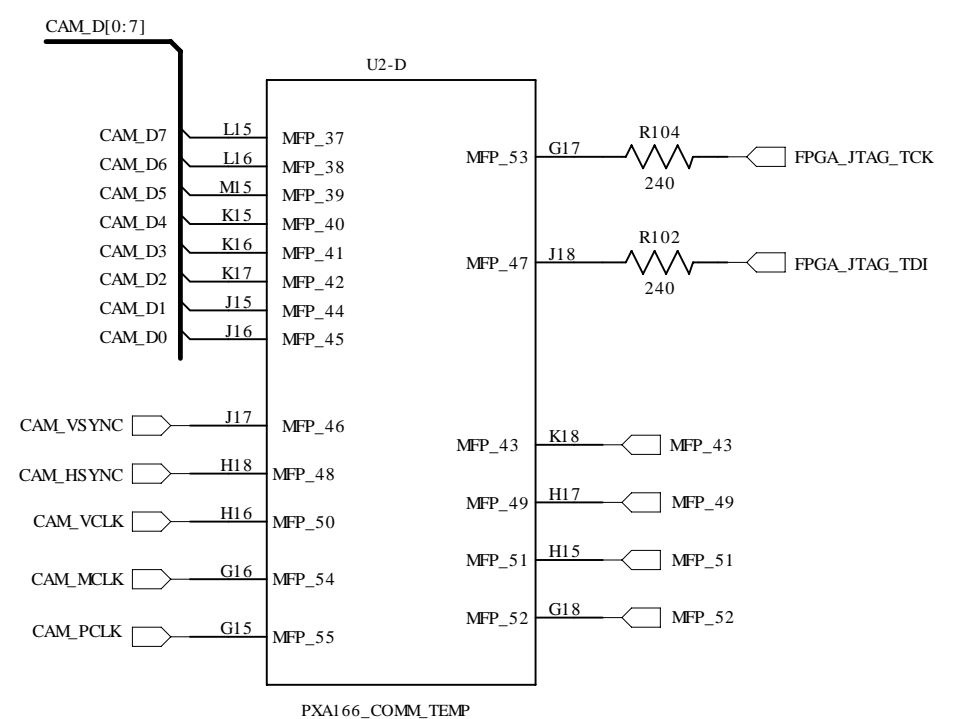
## MMC2



## Control



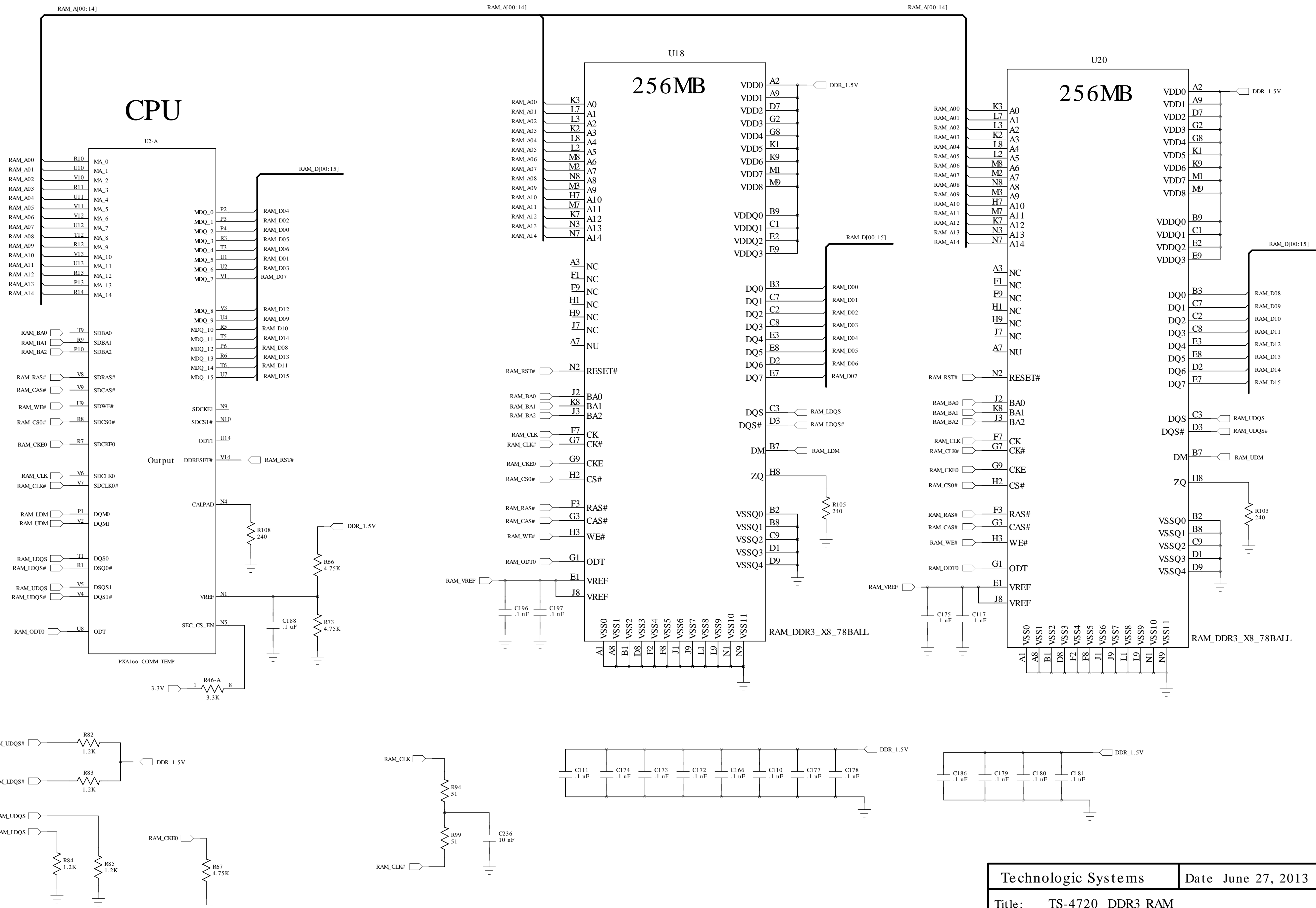
RESET\_IN# is Input only



# DDR3 x8 RAM

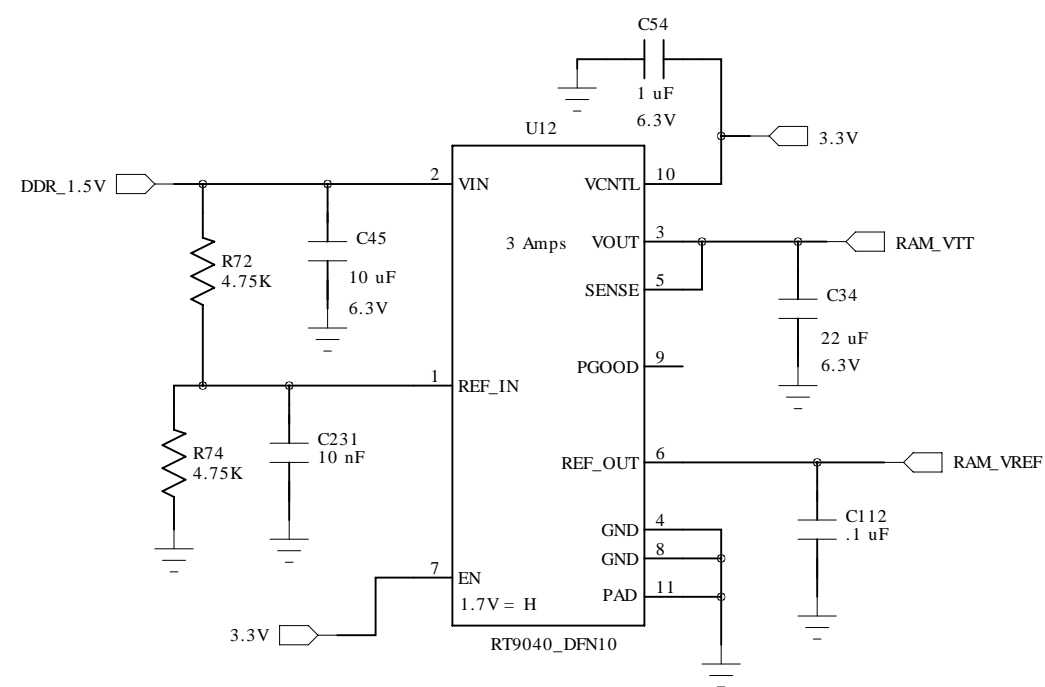
2 Gbit RAM chips

# 512 MB RAM Total

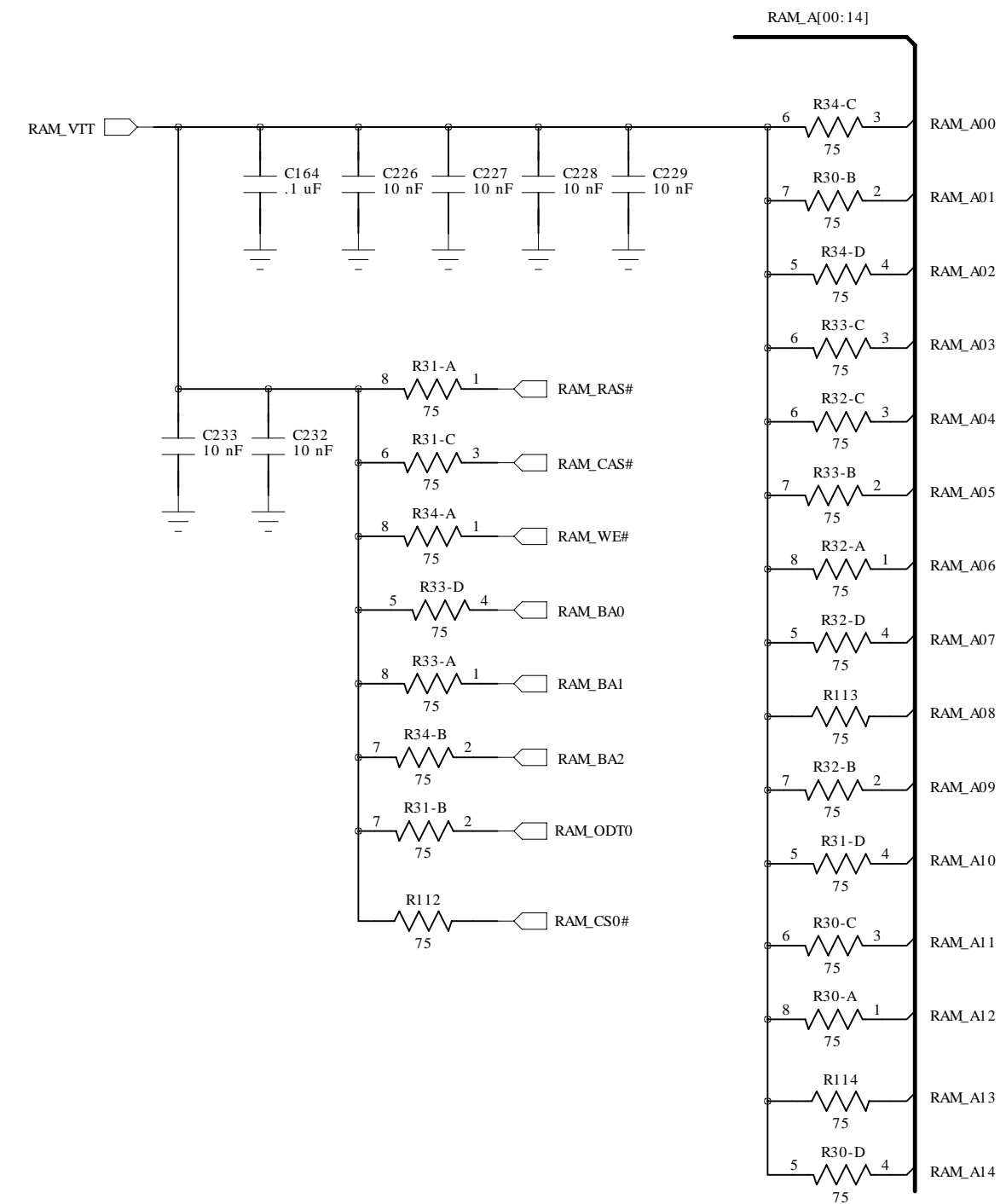


Technologic Systems	Date June 27, 2013
Title: TS-4720 DDR3 RAM	
Rev: A	Designer
Sheet 2 of 10	

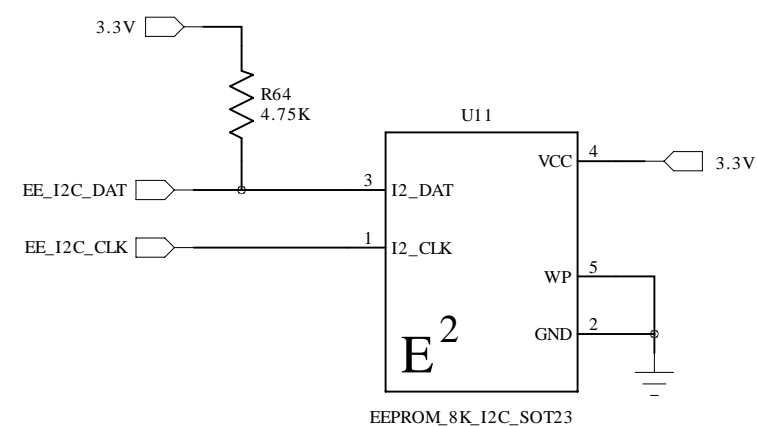
# DDR3 RAM Termination Power Supply



# Termination Resistors



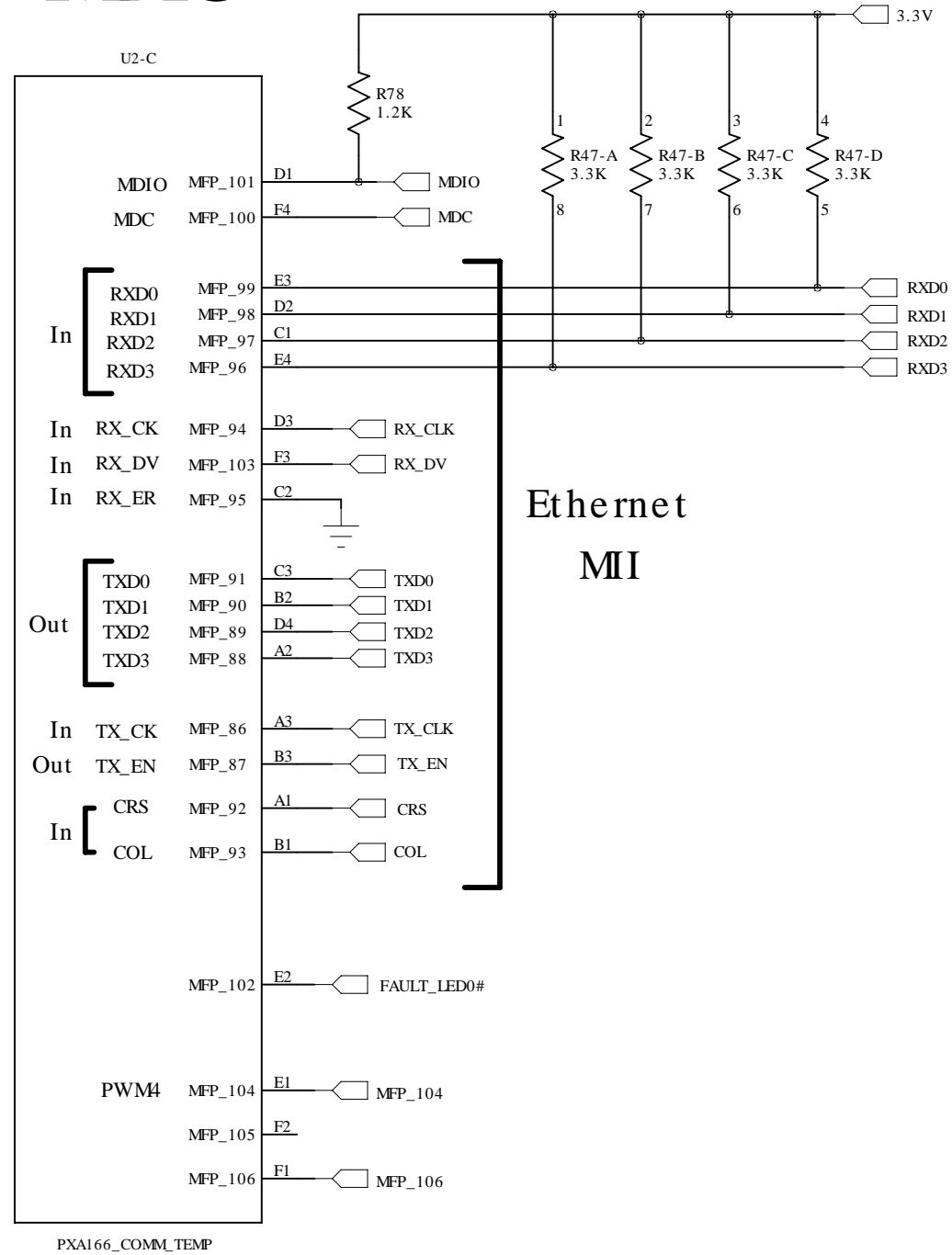
# EEPROM 1 Kbyte



Technologic Systems	Date June 27, 2013
Title: TS-4720 DDR3 Termination	
Rev: A	Designer
Sheet 3 of 10	

# 10/100 Ethernet 4-Port Switch

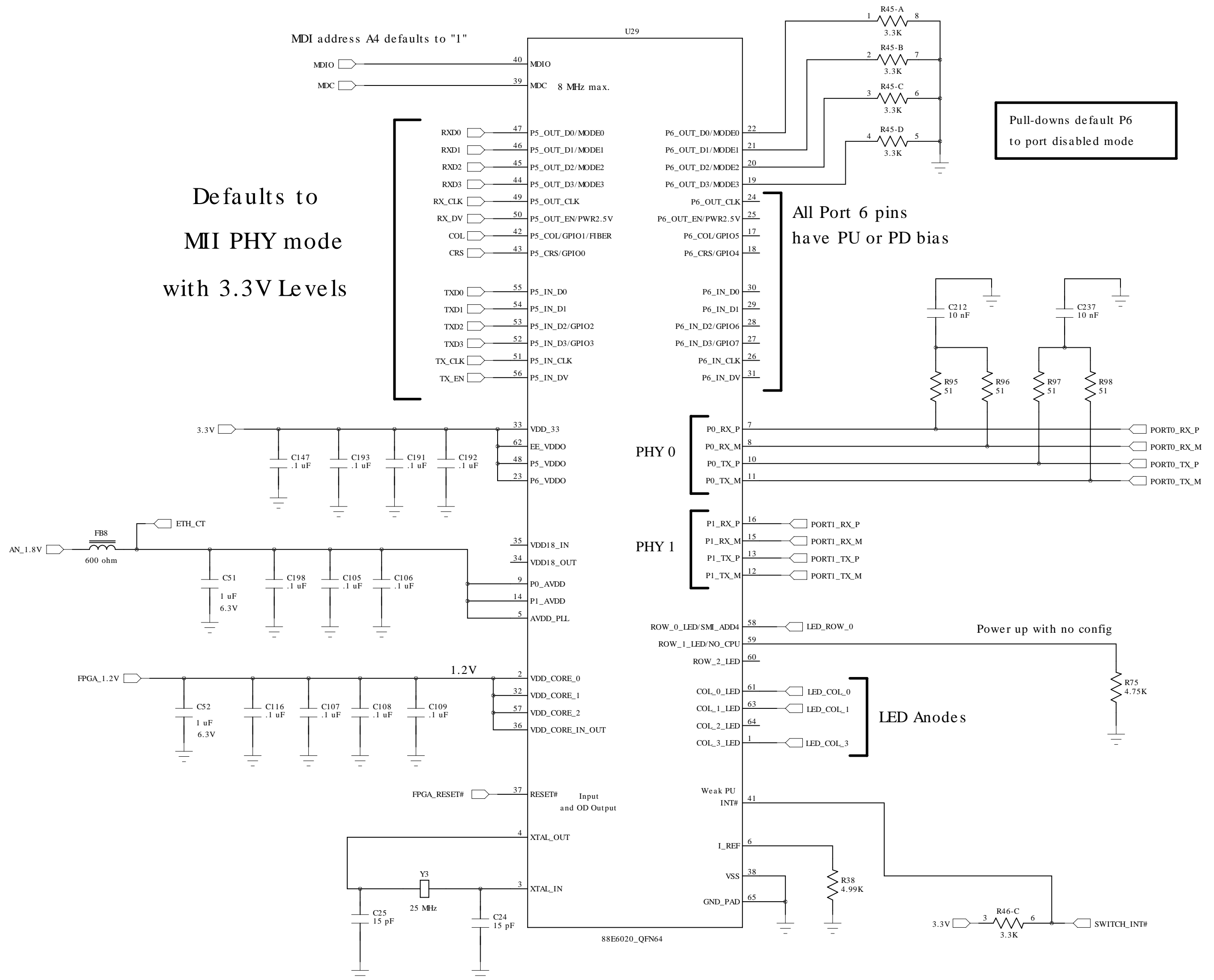
CPU  
MAC



Ethernet  
MII

MDI address A4 defaults to "1"

Defaults to  
MII PHY mode  
with 3.3V Levels



Pull-downs default P6  
to port disabled mode

All Port 6 pins  
have PU or PD bias

Auto MDIX is supported

Polarity Correction also supported

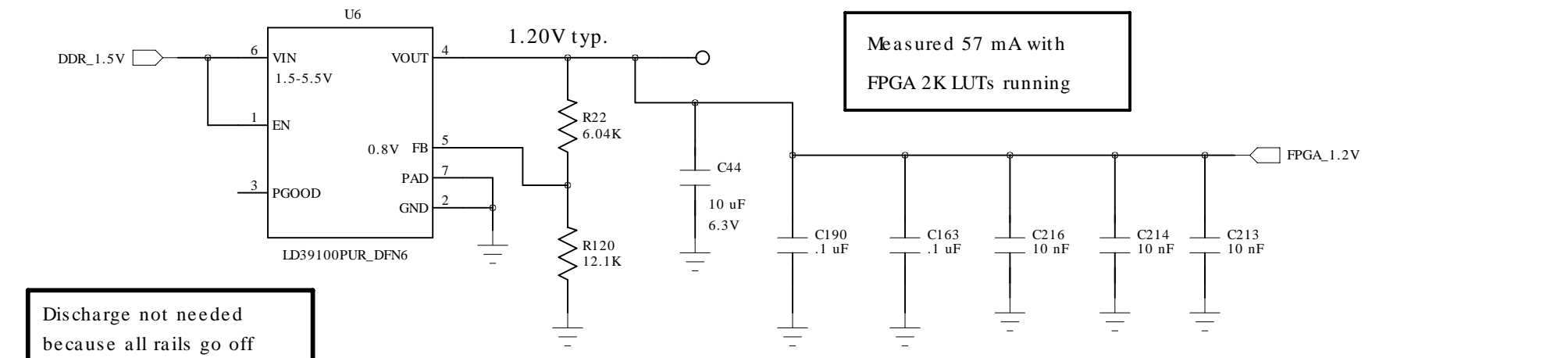
Requires Reset# asserted  
for 10 ms after power

Technologic Systems		Date June 27, 2013	
Title: TS-4720 Ethernet Switch			
Rev: A	Designer RLM	Sheet 4 of 10	

# FPGA with 5K or 8K LUTs

LED Outputs are not OD

## FPGA 1.2V Reg.



Discharge not needed because all rails go off for 200 ms

SMC Bus from CPU

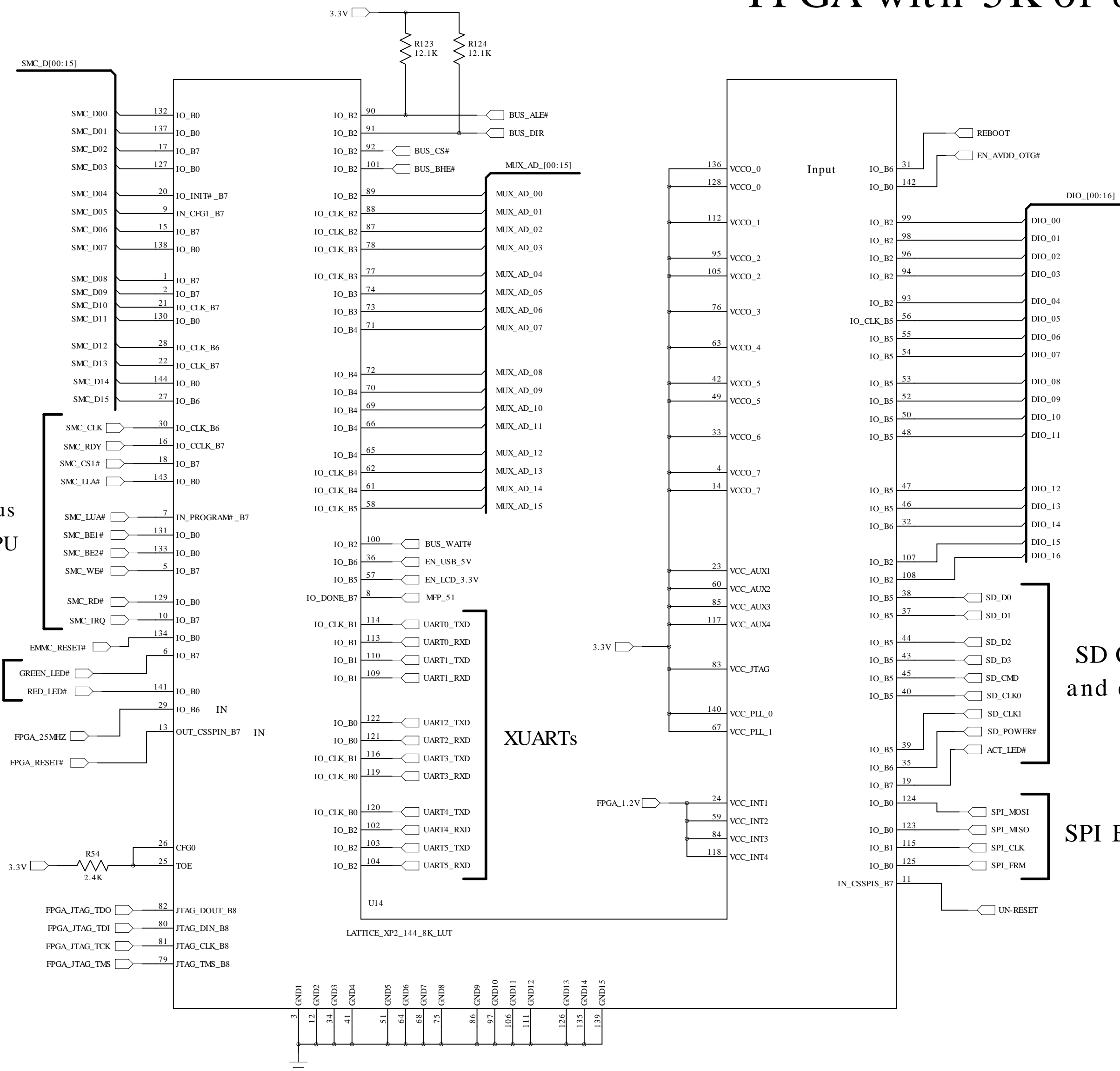
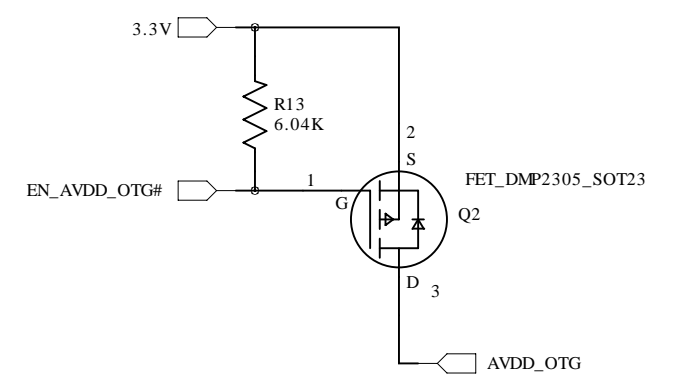
Off Bd. LEDs

XUARTs

SD Card and eMMC

SPI Bus

CPU USB Power



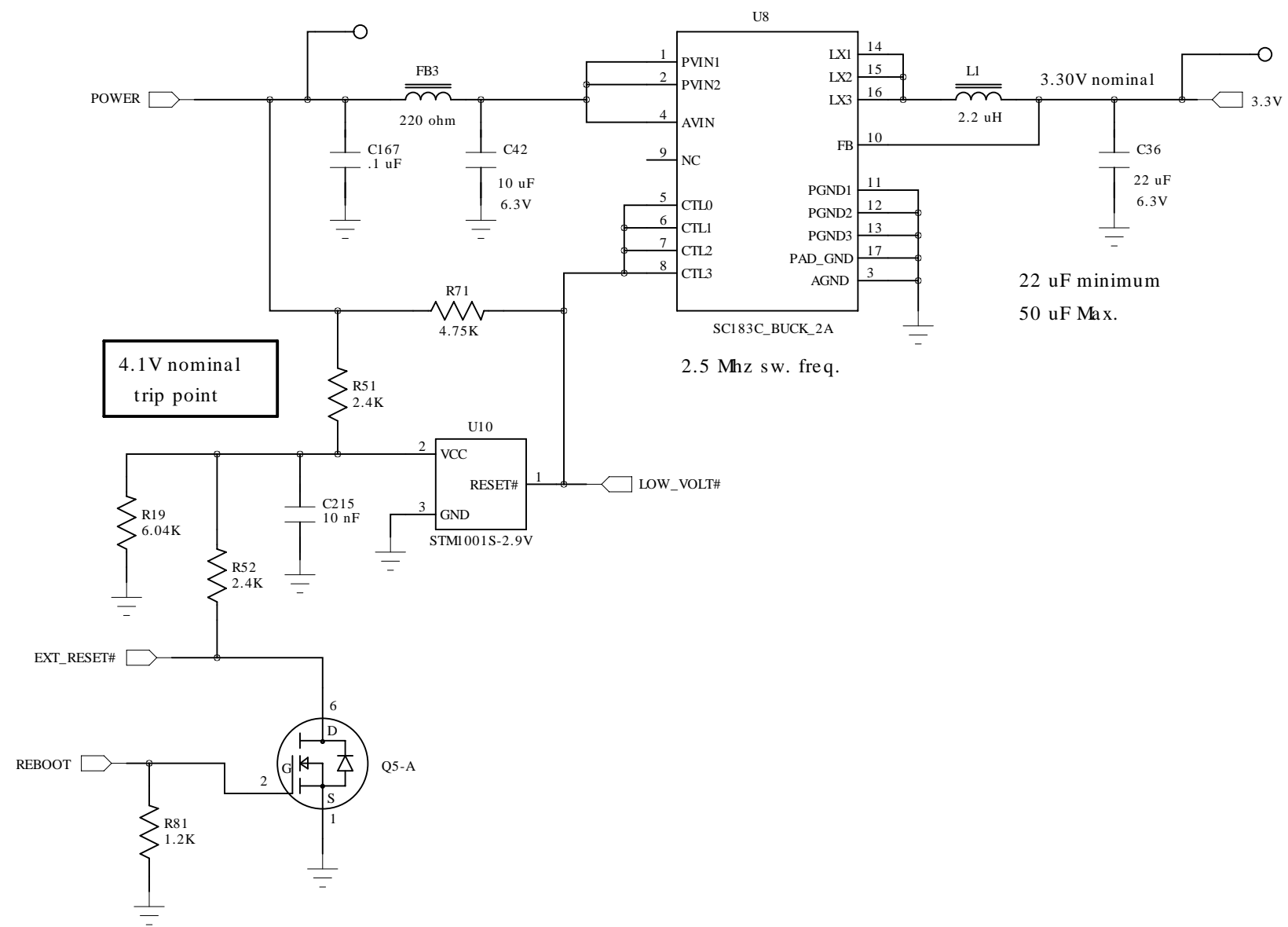
Page 37 of Data Sheet (Hot Socketing)  
Power Supplies can be sequenced in any order but must be monotonic  
All I/O lines are tri-stated during power cycling

Technologic Systems	Date June 27, 2013
Title: TS-4720 FPGA	
Rev: A	Designer
Sheet 5 of 10	

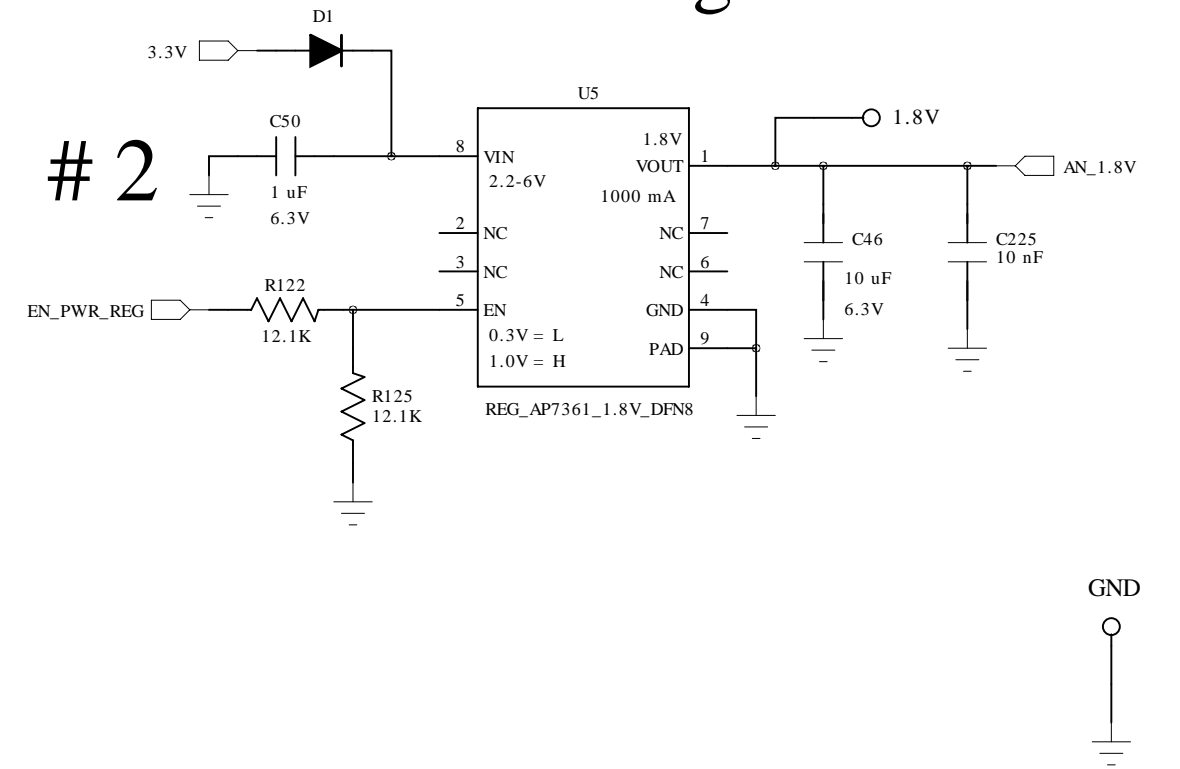
# Power Supplies

## # 1 3.3V Power Supply

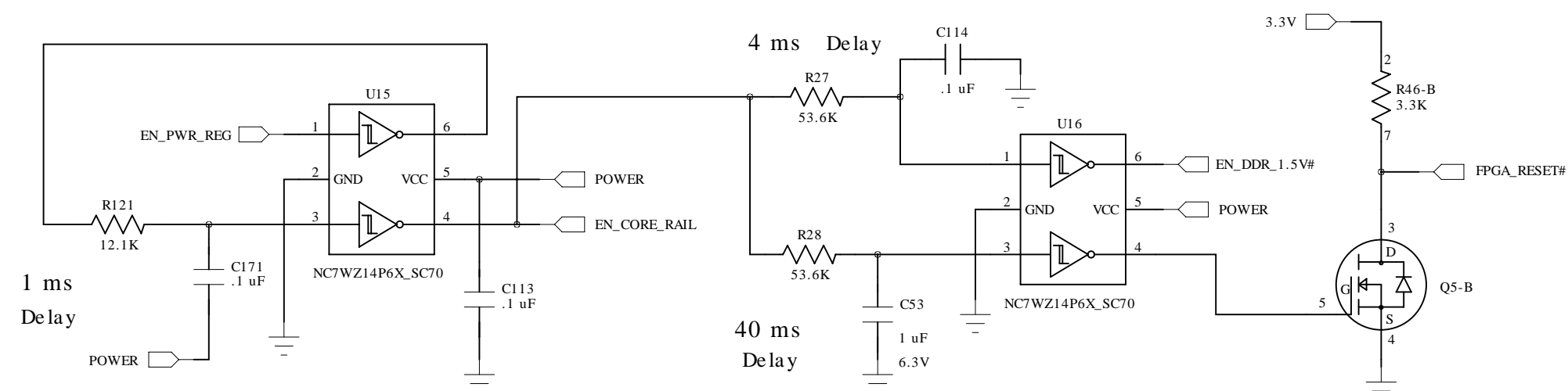
up to 2000 mA



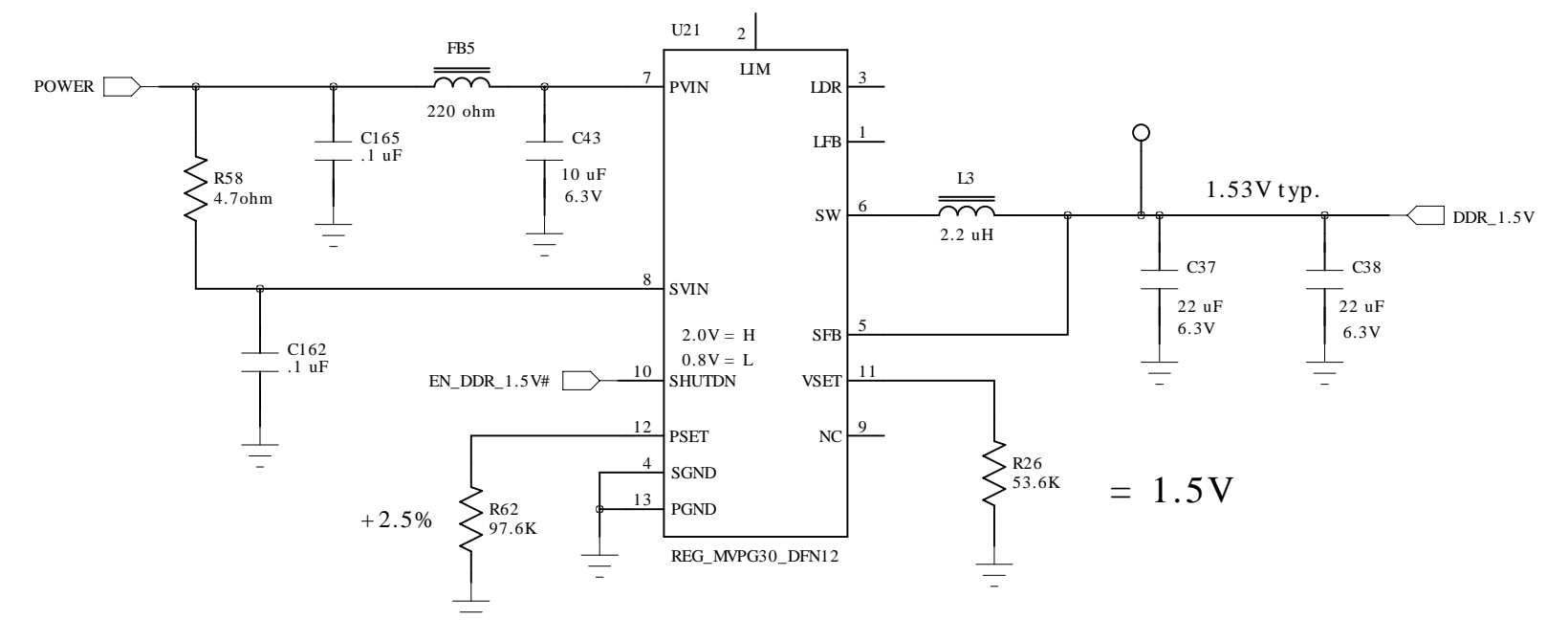
## Analog 1.8V Regulator



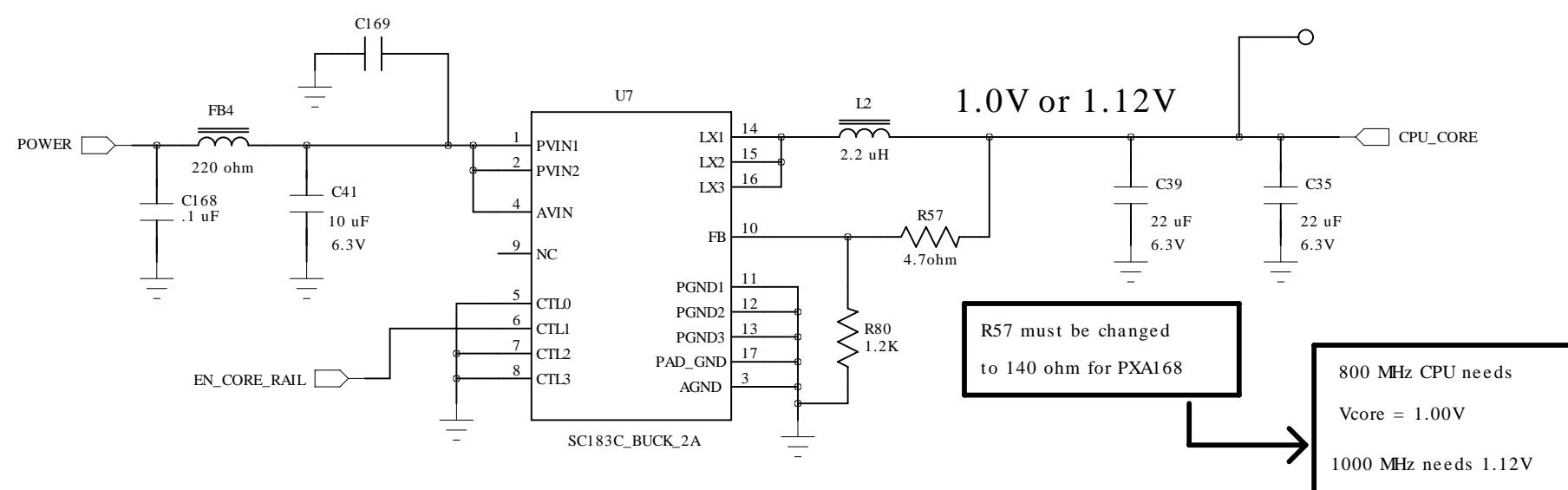
## Power Sequencer



## # 4 DDR3 1.5V Reg.

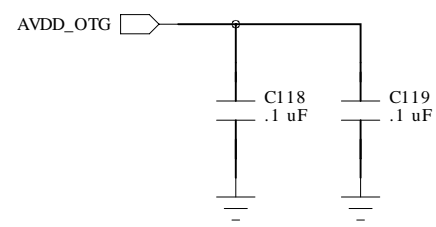
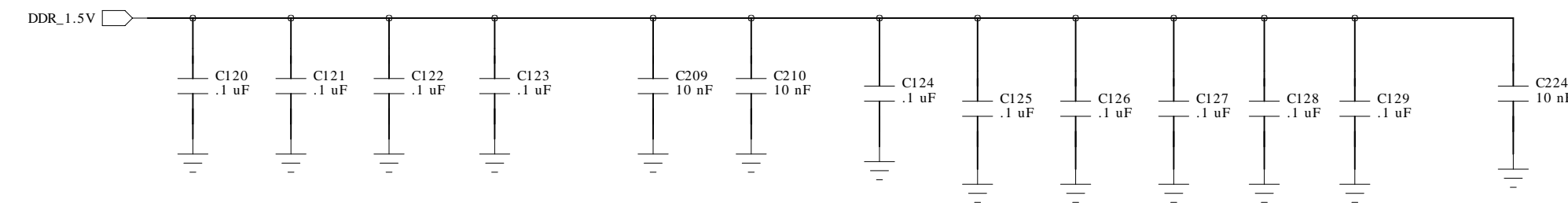
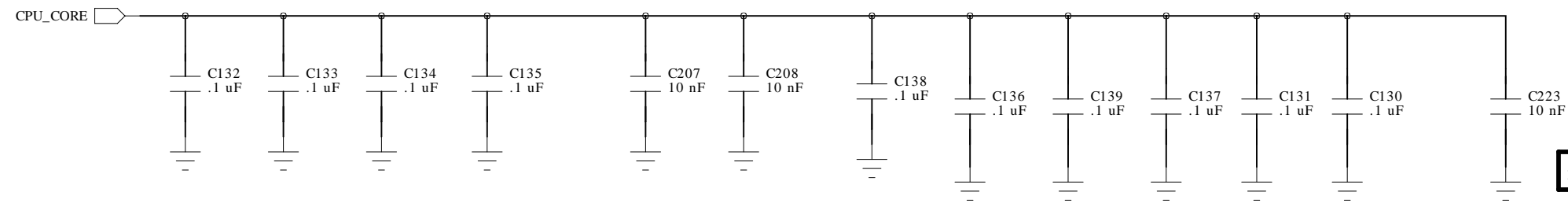
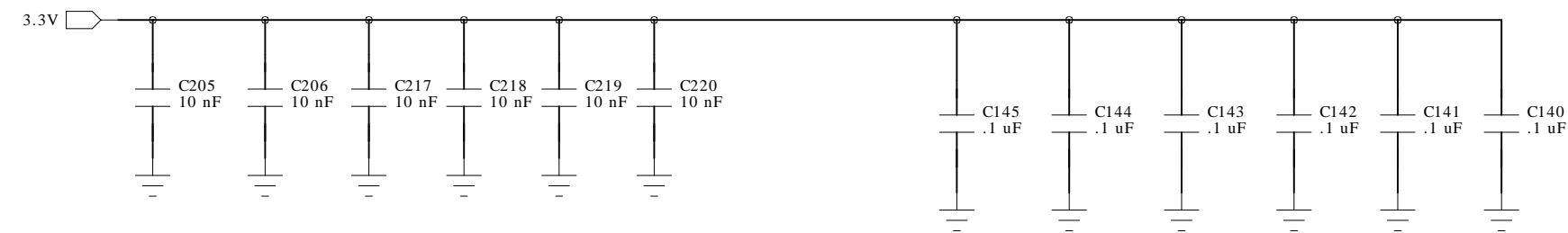
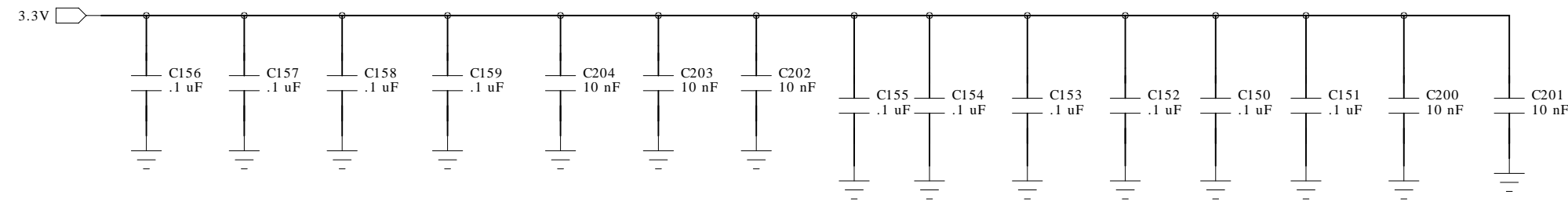


## # 3 CPU Core Supply

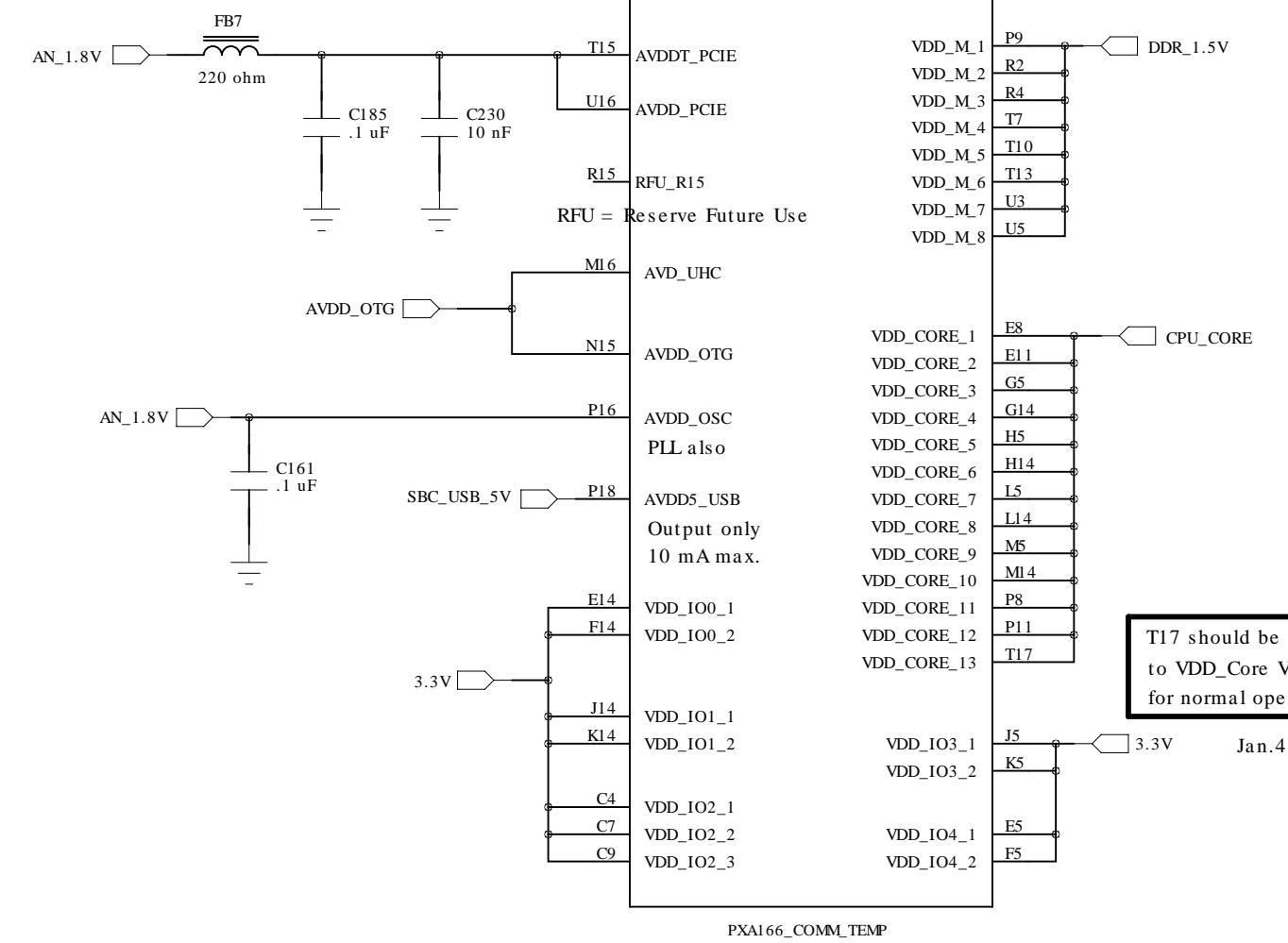


Technologic Systems	Date	June 27, 2013
Title: TS-4720 Power Supplies		
Rev: A	Designer	Sheet 6 of 10

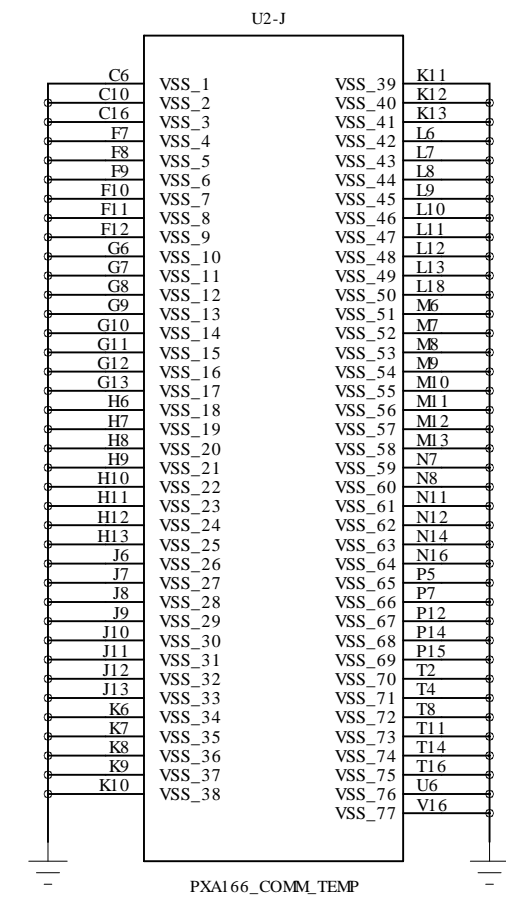
# CPU Power



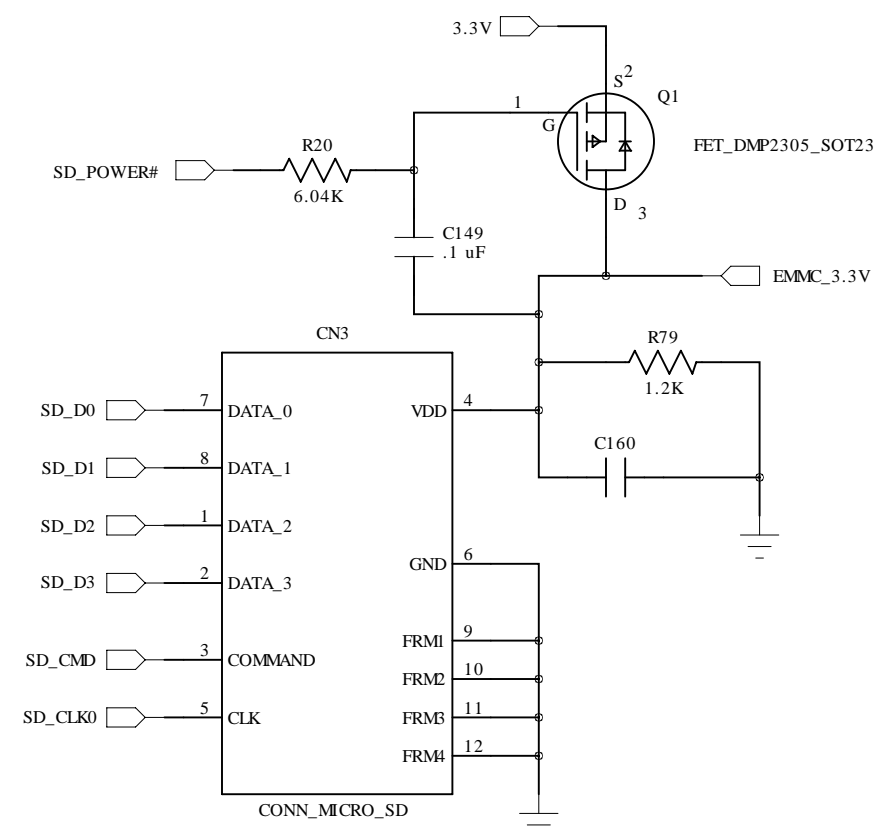
PXA168 PCIe rails must be connected to AN\_1.8V



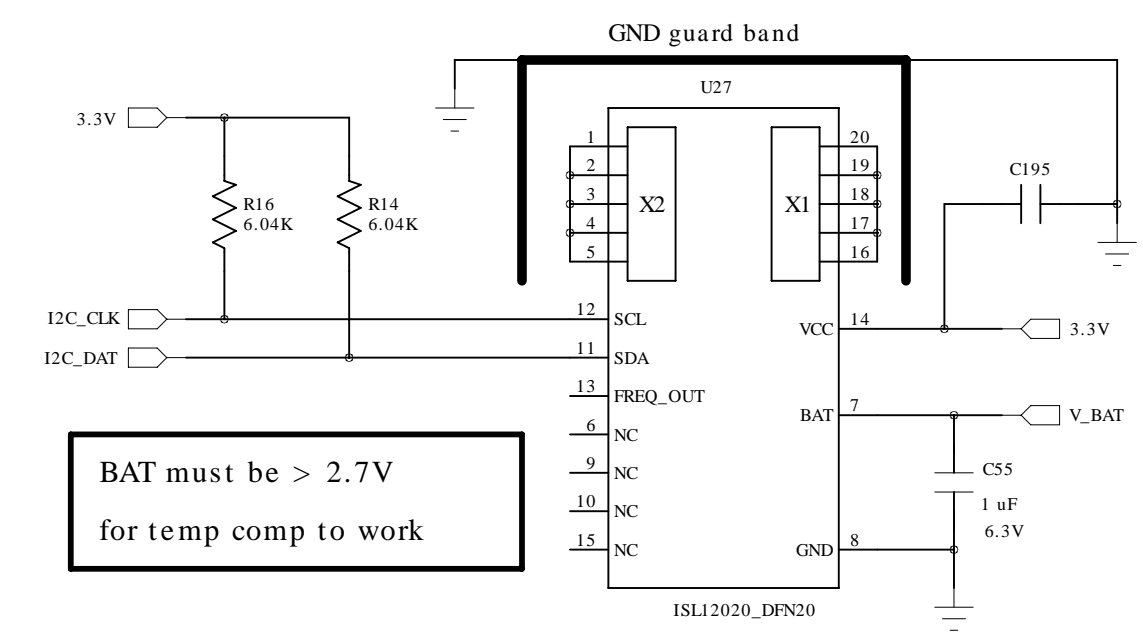
# CPU



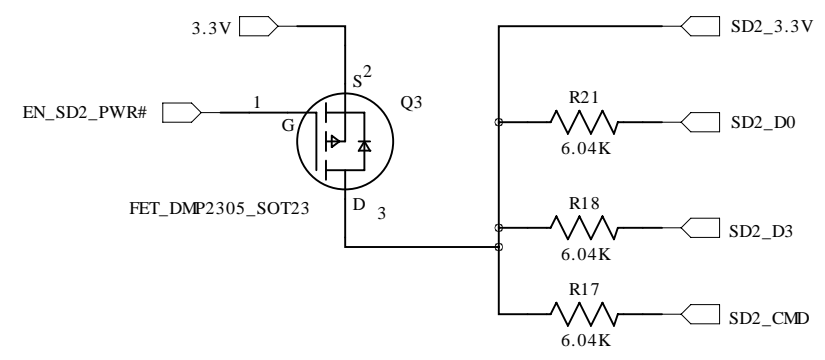
# Micro SD Card Socket



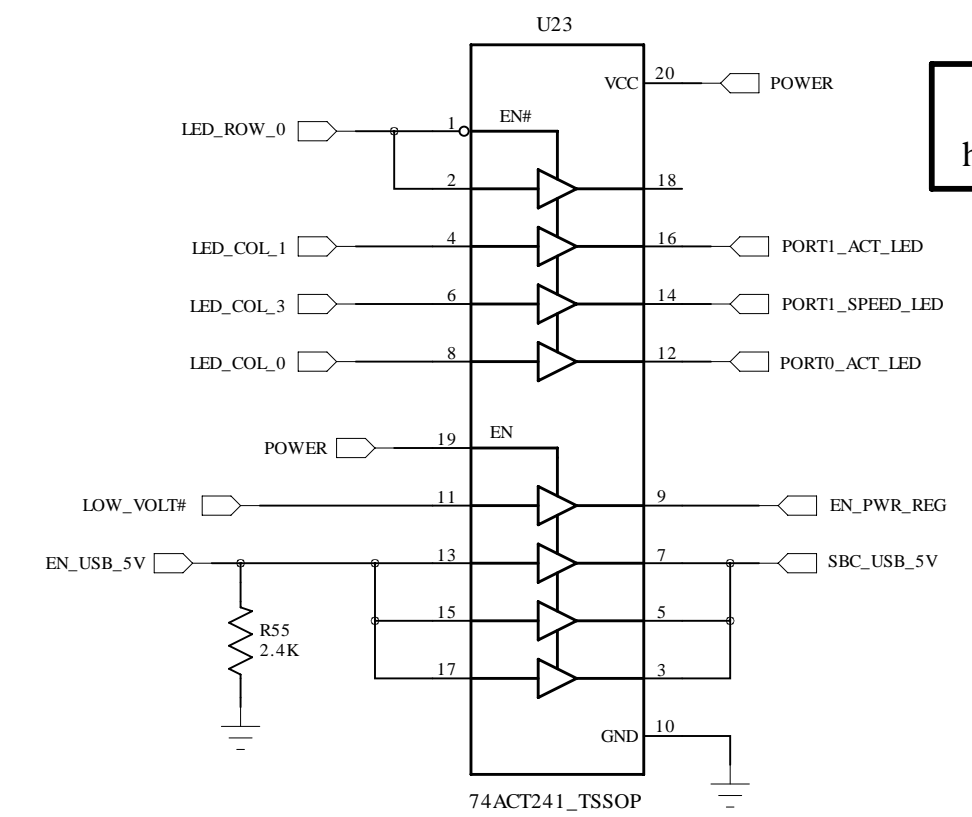
# RTC and Temp. Sensor



# OFF BD. SD Card Power

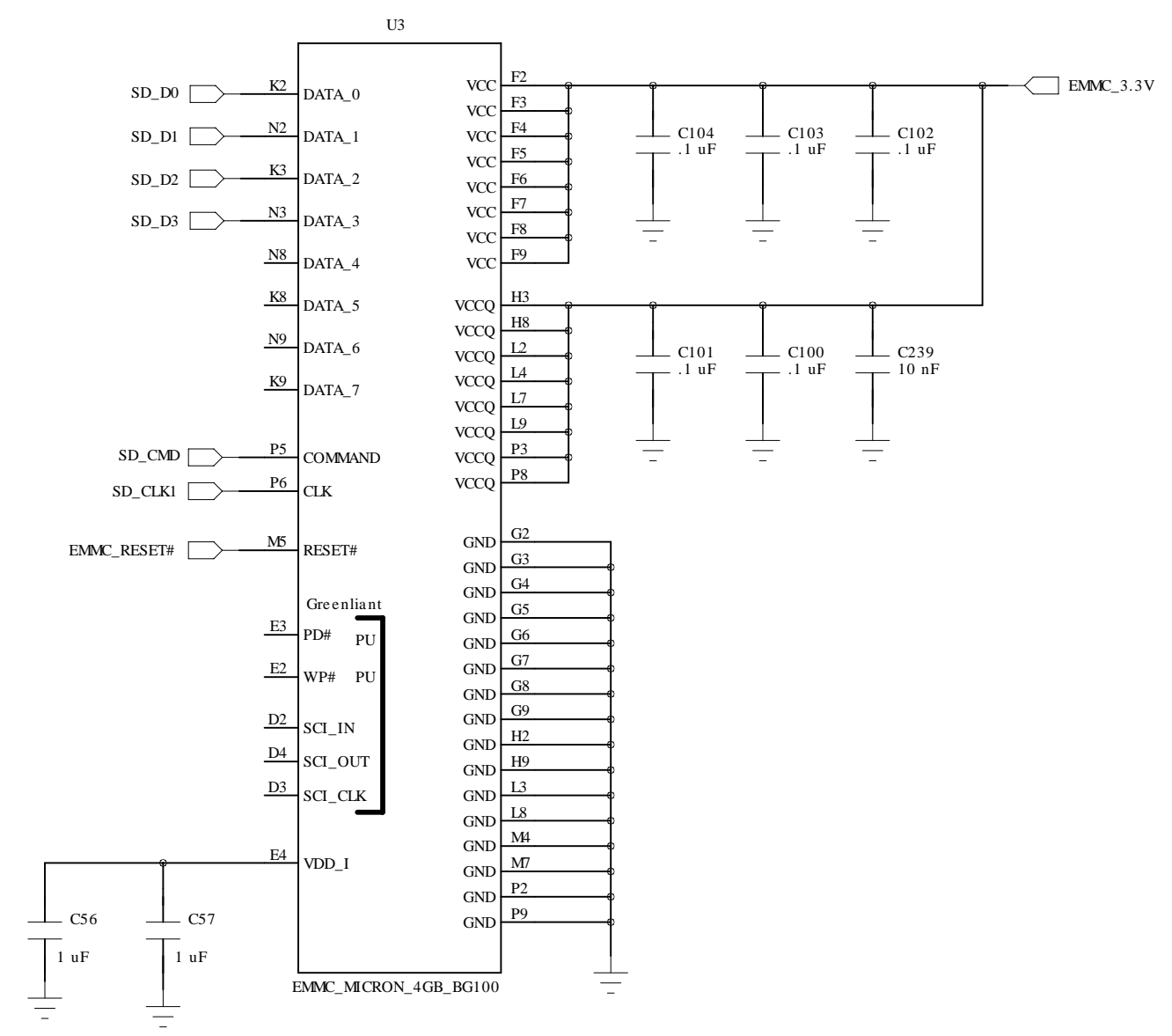


# 3.3V --> 5V Level Shifter

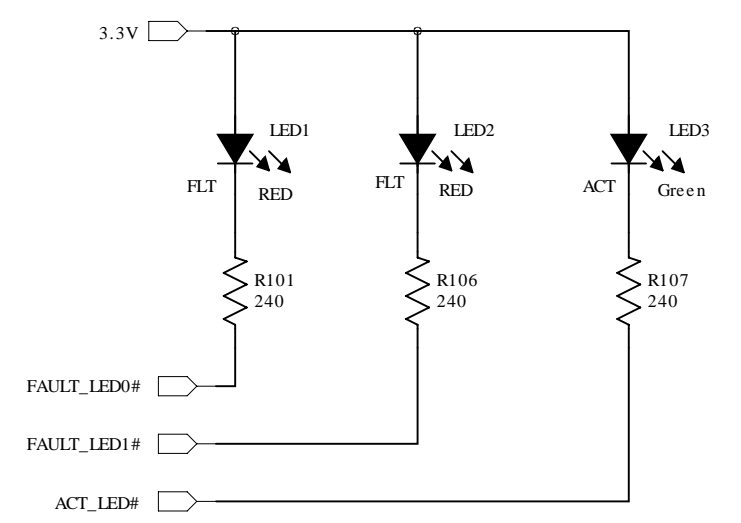


Off-Board LEDs  
have cathode to GND

# eMMC 4GB

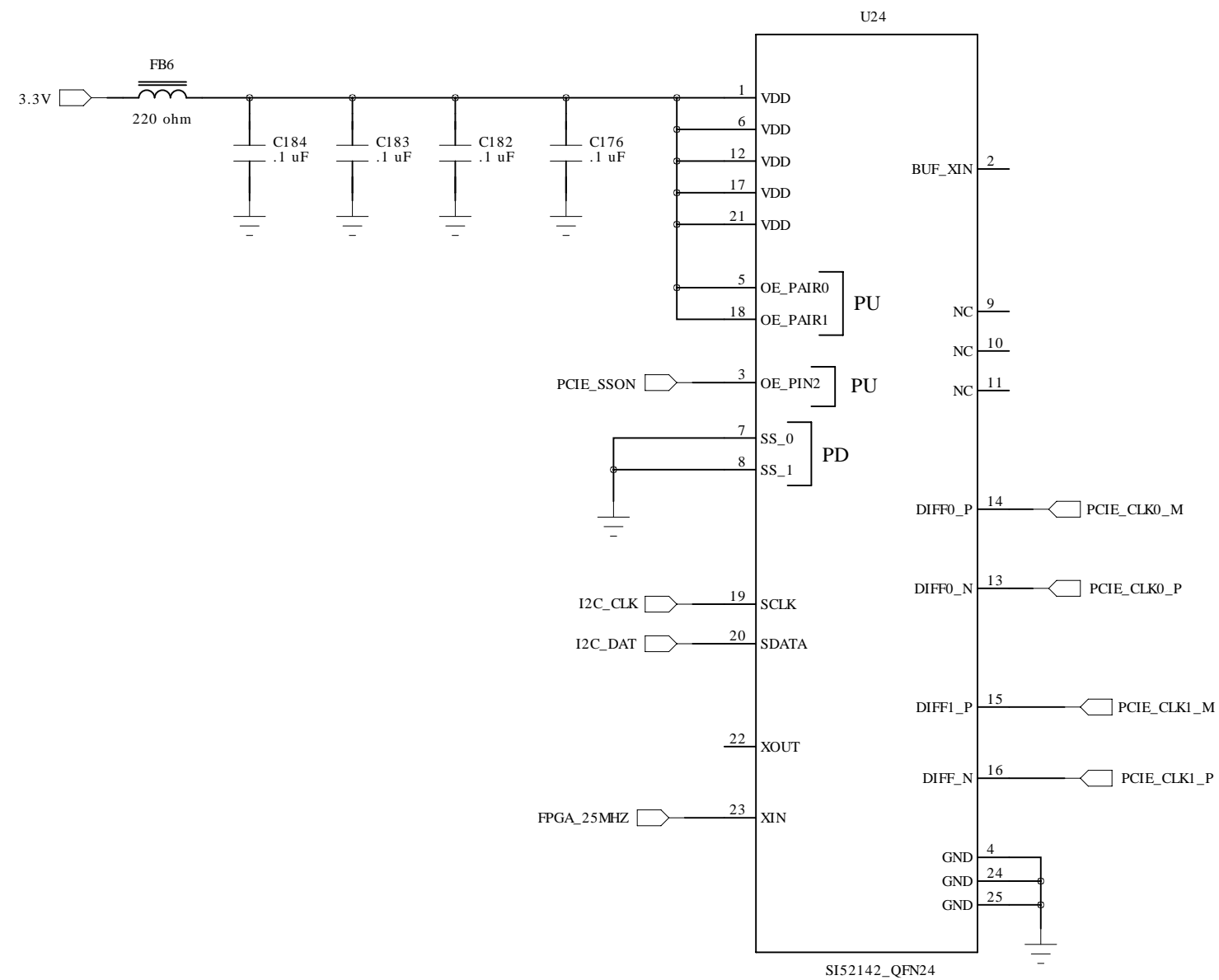


# SD Card LEDs

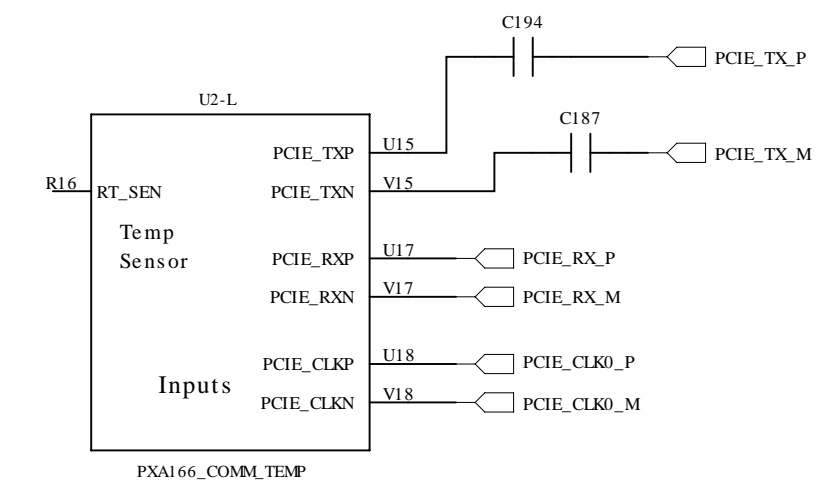




## PCIe 100 MHz Clock Generator

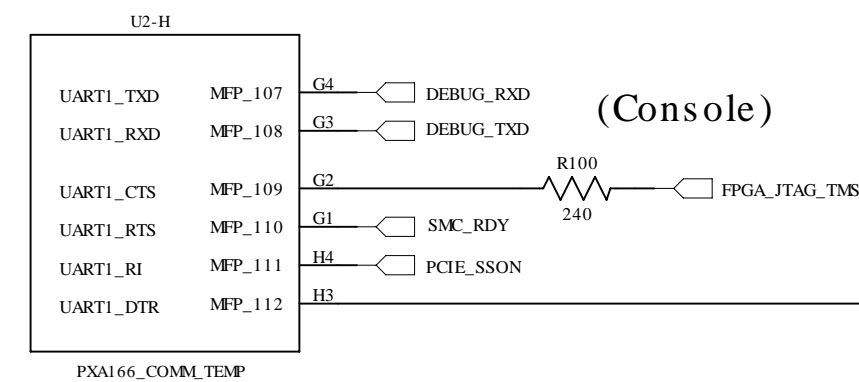


## CPU PCIe

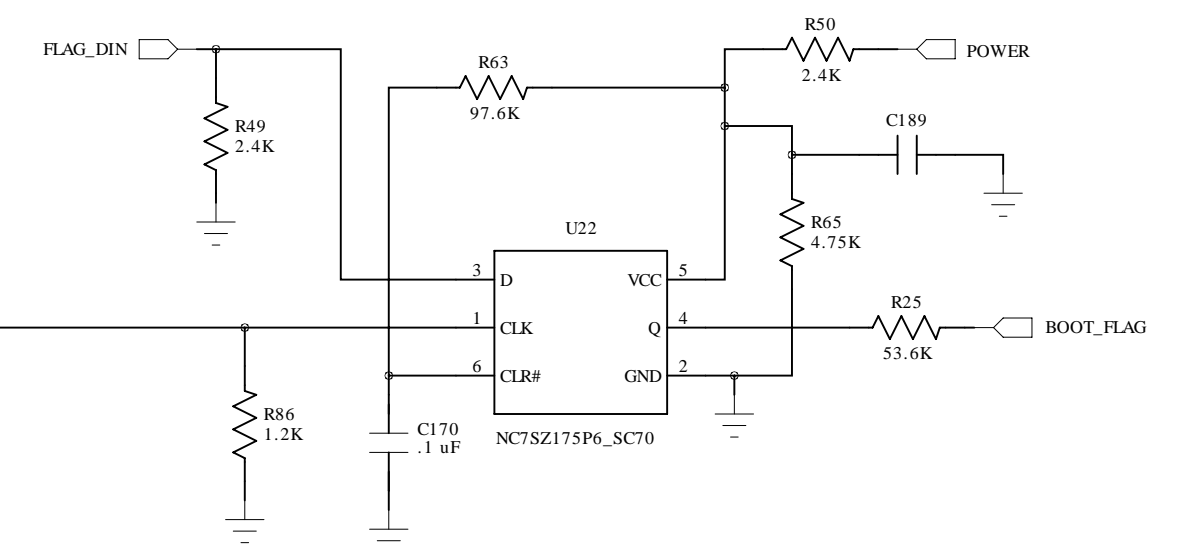


## CPU

### Debug UART



## Reboot Flag



## PXA166 and PXA168 BOM Differences

- R57 = 140 ohm for PXA168
- R56 removed for PXA166
- FB6, FB7 removed for PXA166
- U24 removed for PXA166
- U2 = PXA166 Commercial Temp  
or = PXA168 Industrial Temp

# Two 100-pin Off-board Connectors

"POWER" pins supply all power to the module  
Apply 4.5V to 5.5V to these pins  
Current drain is approximately 400 mA

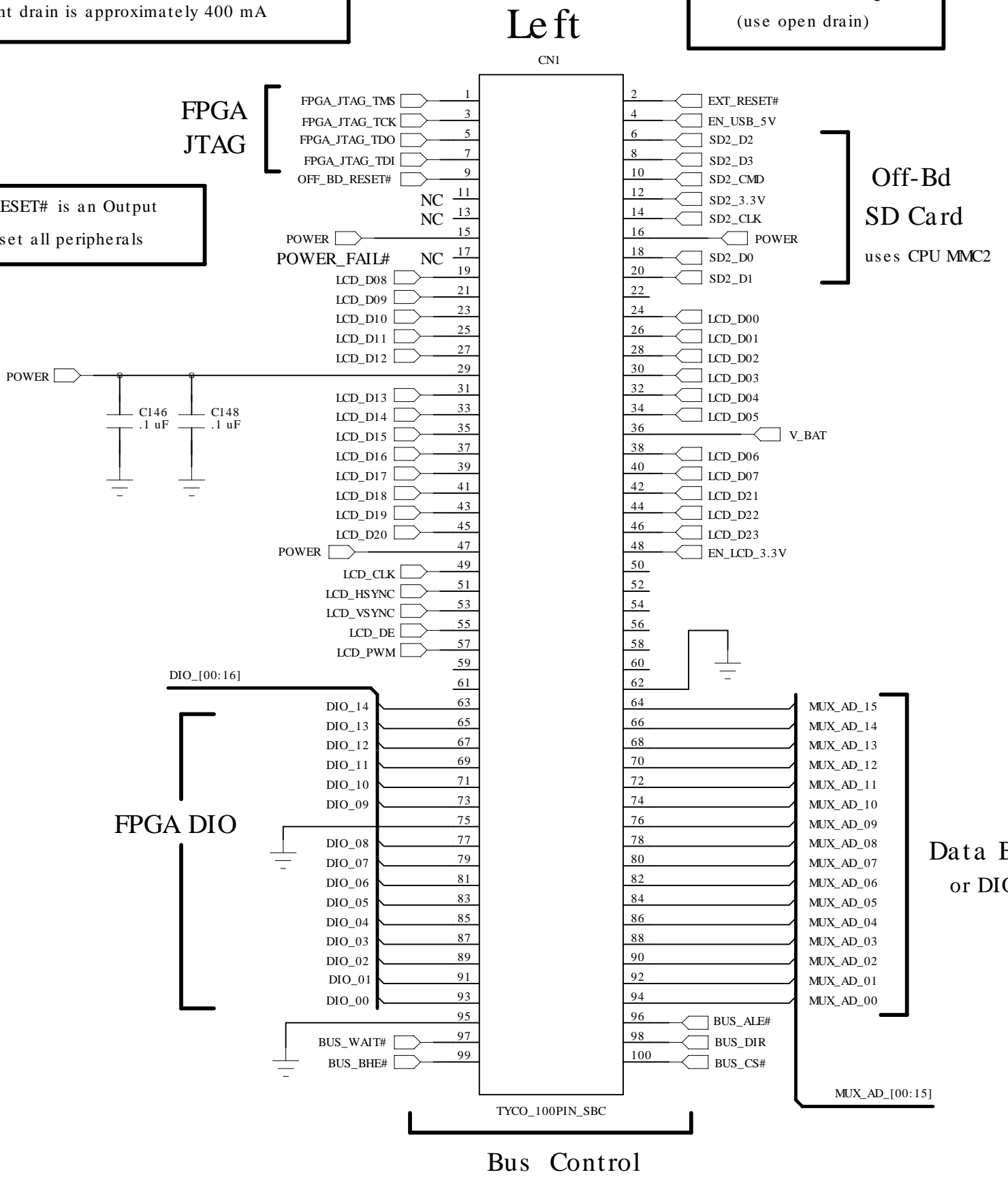
EXT\_RESET# is an Input  
used to reboot the CPU  
Do not drive active high  
(use open drain)

Must have 10 nF Capacitor  
very near CN2 and GND  
for all "quiet" signals  
(between diff pairs)

Pin 1 is the top left corner pin on the  
connector. All of the pins on the left  
are odd numbered. This may differ from  
the connector manufacturer's datasheet.

All signals driving DIO on CN1 &  
CN2 must be powered by the  
3.3V on CN2, or remain at 0V until the  
CN2 3.3V rail is > 3.0V

OFF\_BD\_RESET# is an Output  
used to reset all peripherals



Any I/O routed to a user accessible  
connector should have additional ESD  
protection placed on the carrier board.

If Bus is not needed, all Bus  
signals can be changed to DIO

- Devices connected to this bus must never drive it when BUS\_CS# is deasserted (must be off within 30 nS of deassertion)
- Devices must pull the BUS\_WAIT# line low if they need more than 150 nS strobe
- The data bus can not have more than 30 pF of off-board capacitive loading  
May need data buffer chip for heavy loads

3.3V rail can supply up  
to 700 mA to base board

Maximum off-board load  
on AN\_1.8V is 10 mA

Max. load on JTAG\_Vcc  
(CN2-79) is 20 mA  
Not always 3.3V

