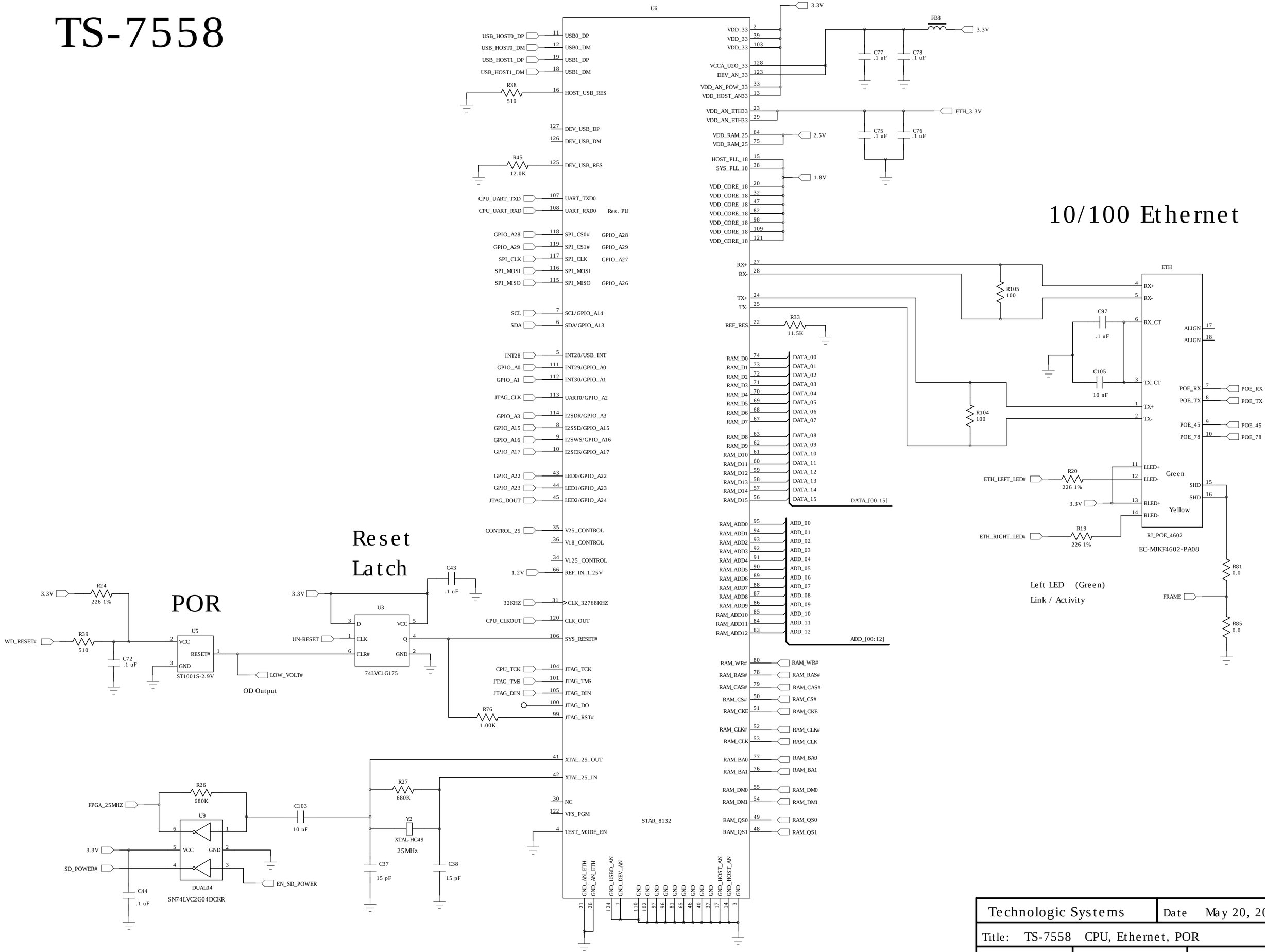
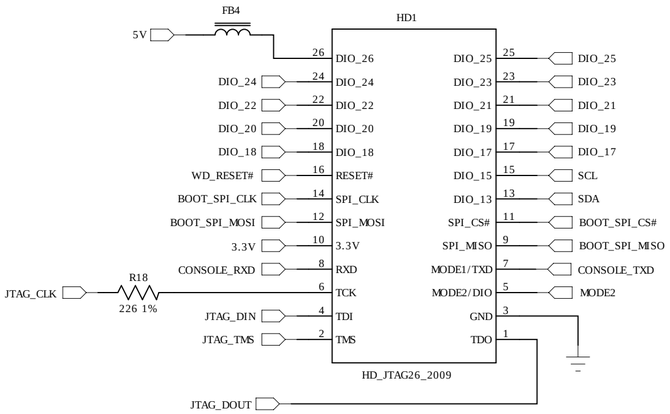
TS-7558



Technologic Systems	Date May 20, 2011	
Title: TS-7558 CPU, Ethernet, POR		
Rev: A	Designer	Sheet 1 of 12

JTAG 26-pin Header



Mode 1	Mode 2	Boots from
1	1	NAND Flash
1	0	SD Card
0	1	Off-board Flash
0	0	Off-board Flash

MODE1 and MODE2 states are latched when CPU_RESET# is deasserted

MODE1 and MODE2 have 4.7K resistor pull-ups on WM-7550

Use 680 ohm resistor to GND to set low

Console always is enabled

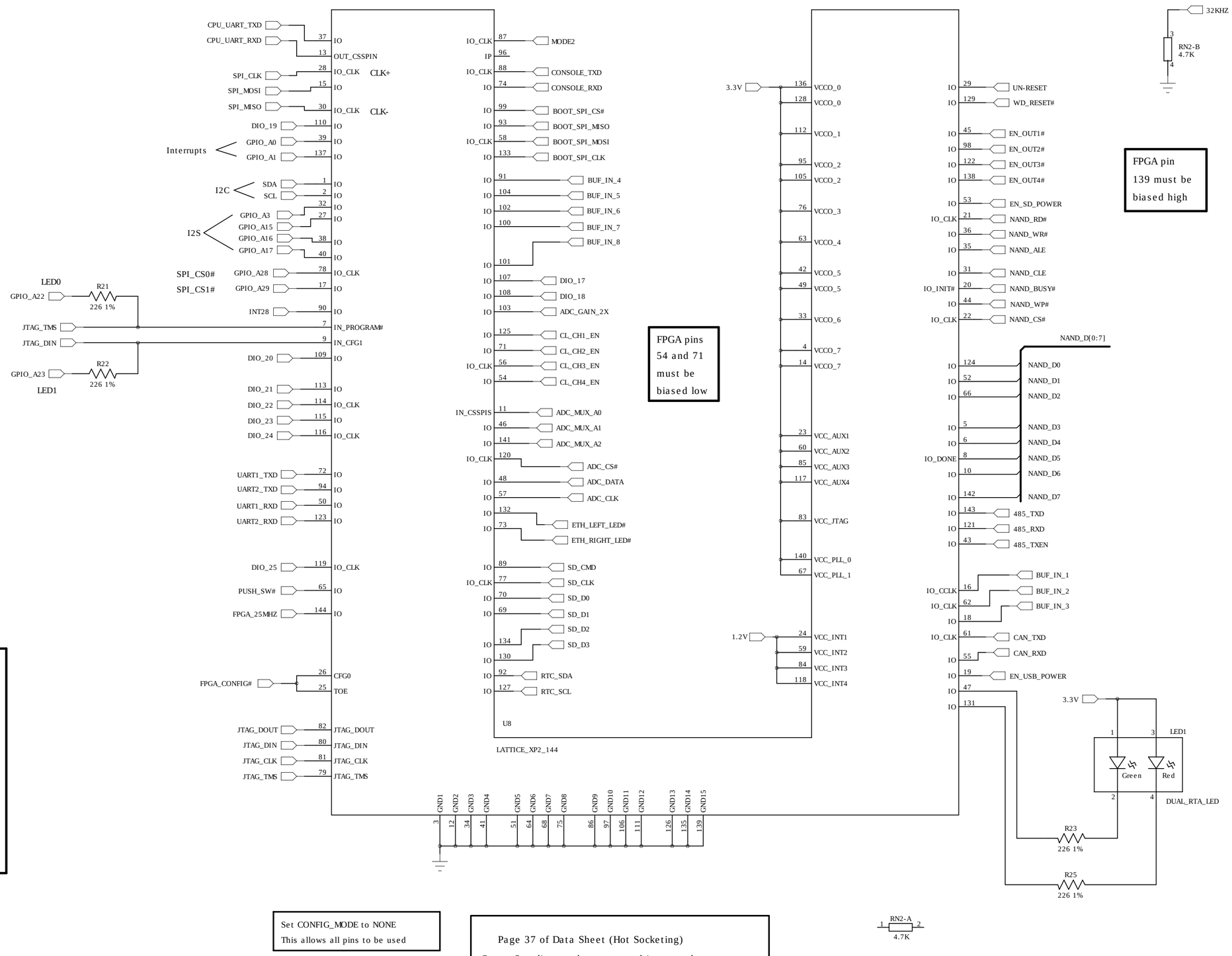
Board ID bits

	Pin 54 (weak PU)	Pin 138 (weak PD)	Pin 71	Pin 37	Hex
TS-7500	1	1	1	1	F
TS-7550	1	1	0	1	B
WM-7551	0	0	1	1	C
TS-7552	1	0	1	1	D
TS-7553	1	0	0	1	9
TS-7554	0	0	0	1	8
TS-7558	0	1	0	1	A
TS-4500	0	0	0	0	0

7552 and 7553 FPGA pin 93 = MISO

FPGA with 5000 LUTs

XP2-5 has:
5K LUTS 2 PLLs
9 blocks of 1Kx18 Block RAM
12 18x18 Multipliers
100 I/O with 144 pin package
"instant ON" = about 1.5 mS
input PLL clock = 10 MHz min



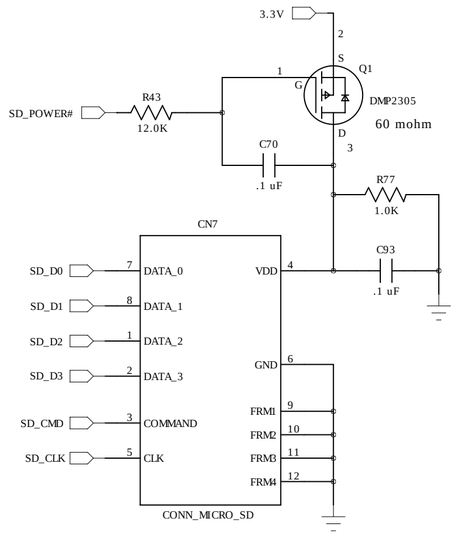
Set CONFIG_MODE to NONE
This allows all pins to be used

Pull-up and pull-down resistors are 6 to 30K ohms

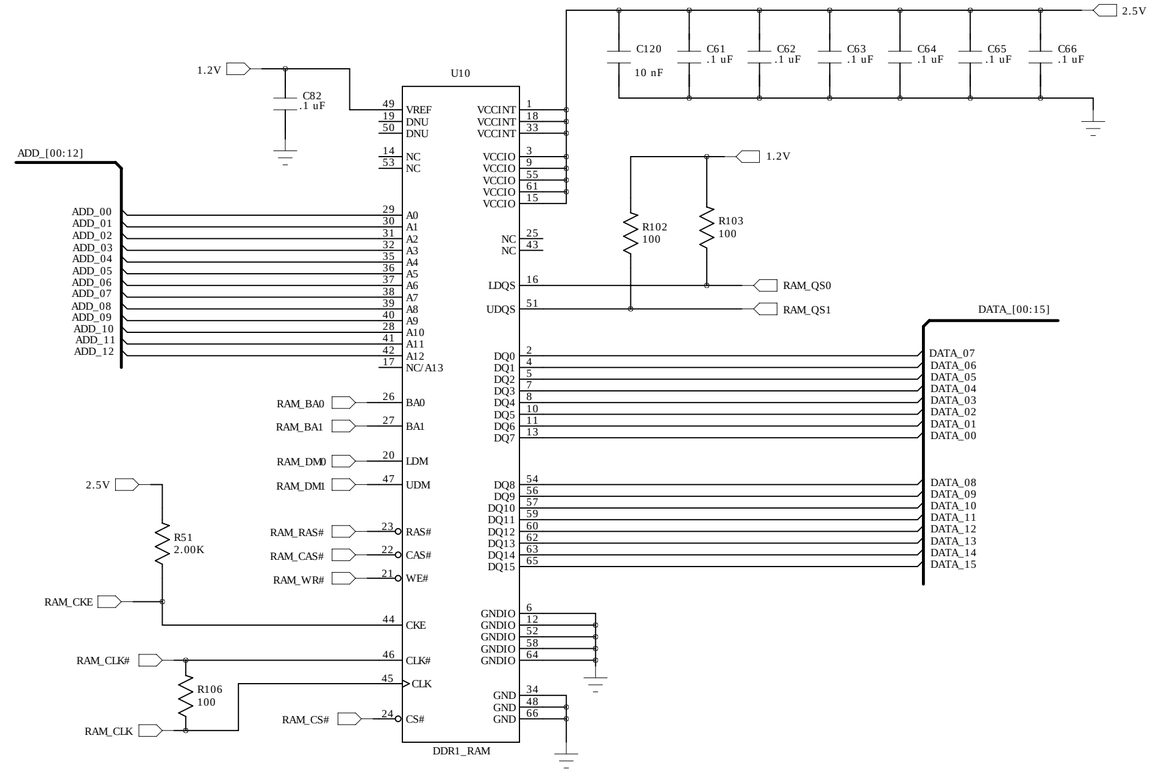
Page 37 of Data Sheet (Hot Socketing)
Power Supplies can be sequenced in any order but must be monotonic
All I/O lines are tri-stated during power cycling

Technologic Systems		Date May 20, 2011
Title: TS-7558 FPGA, JTAG Header		
Rev: A	Designer RLM	Sheet 2 of 12

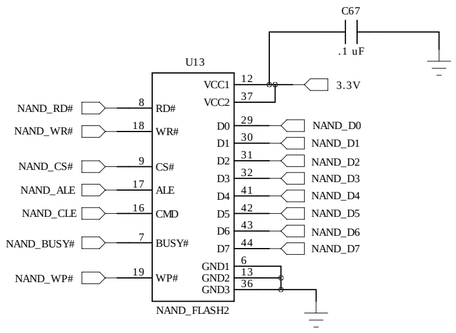
Micro SD Card Socket



64 Mbyte
DDR1 SDRAM



512 Mbyte
NAND Flash



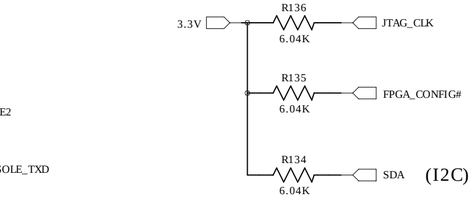
DDR RAM Notes

The DDR clock differential pair is the most critical trace on the entire board

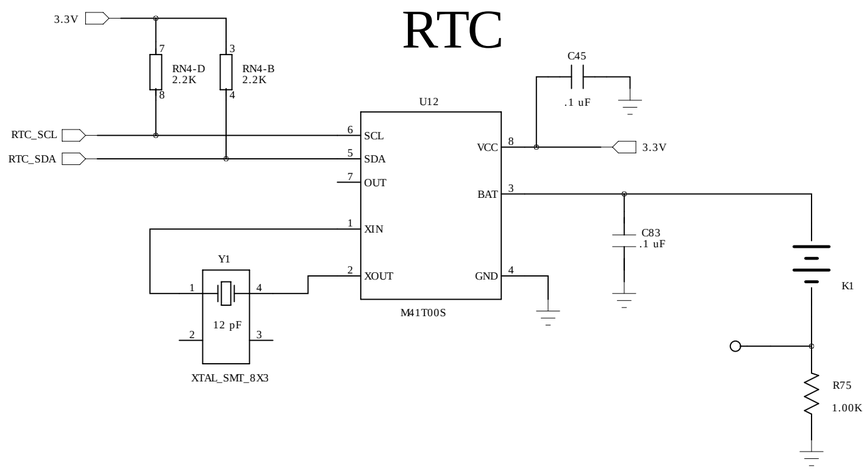
The data lines in each byte lane can be swapped on the RAM chip for optimal layout
Example: D0 and D5 can be swapped, but not D7 and D8

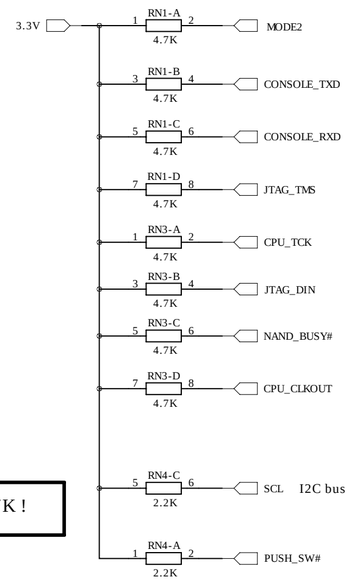
The trace length of each data line (in a single byte lane) and the respective
QS and DM signals must be matched to within 2.5 mm

Address and Command signals can be grouped together, but must be isolated
from data and M_DSQ and M_DM signals (by at least .5 mm)
Or run them on different layer

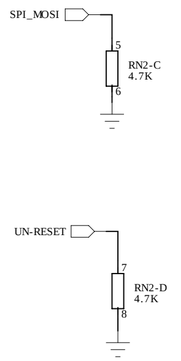


RTC



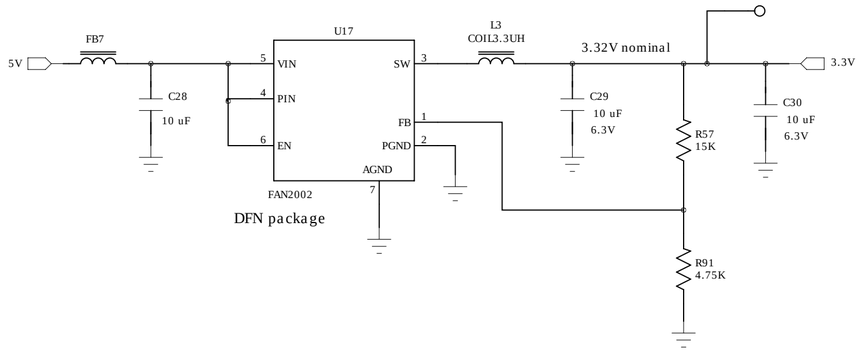


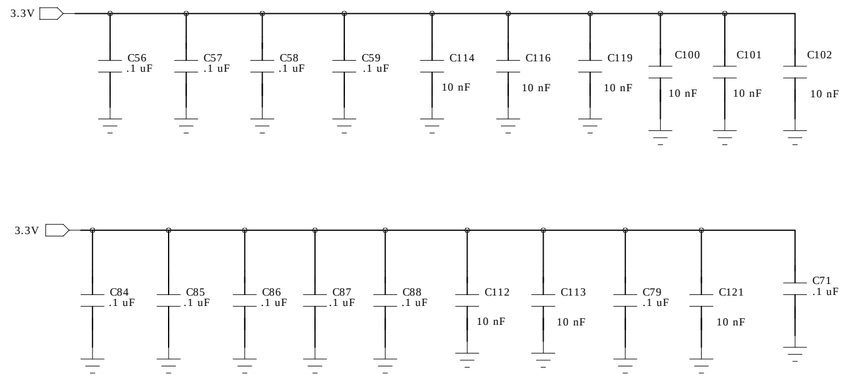
RN4 is 4.7K !



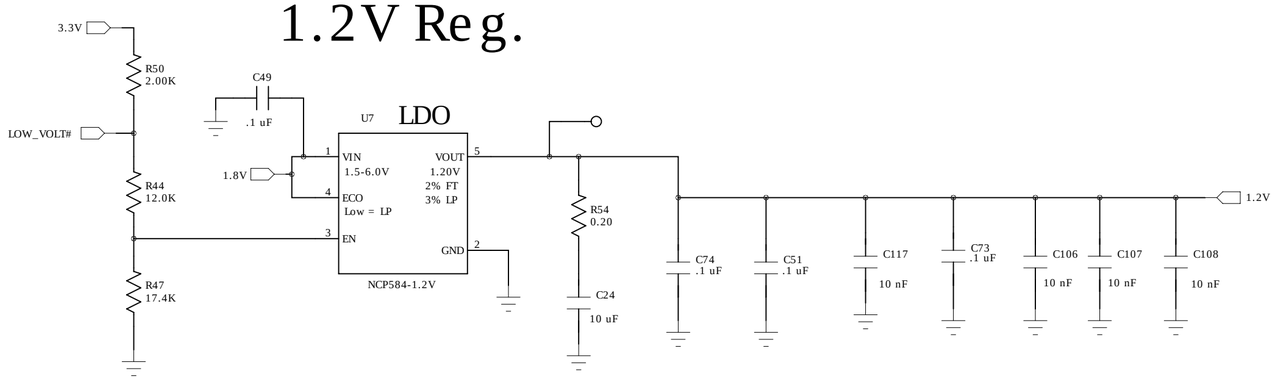
Technologic Systems	Date May 20, 2011	
Title: TS-7558 RAM, RTC, Flash, SD card		
Rev: A	Designer	Sheet 3 of 12

3.3V Regulator

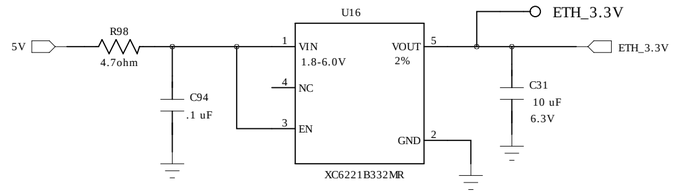




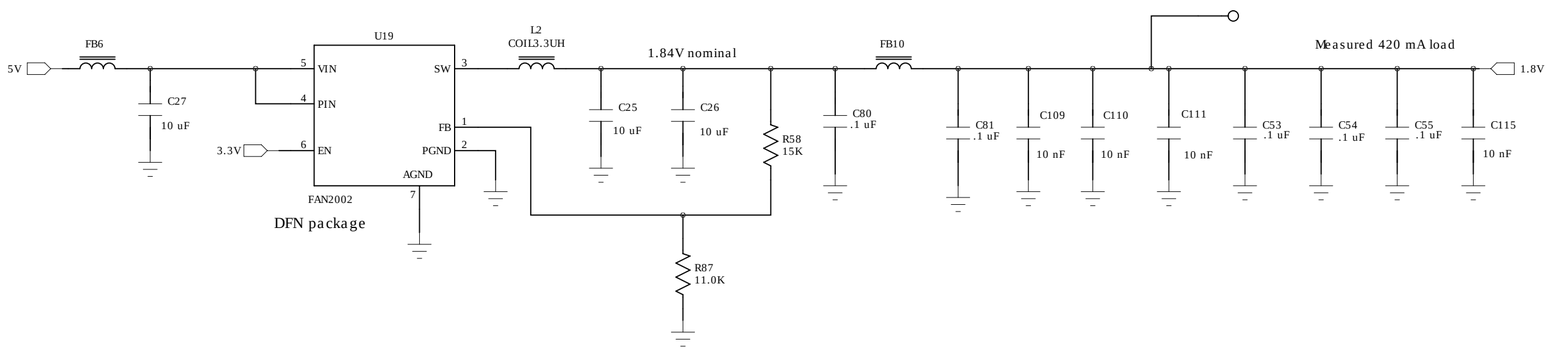
FPGA Core 1.2V Reg.



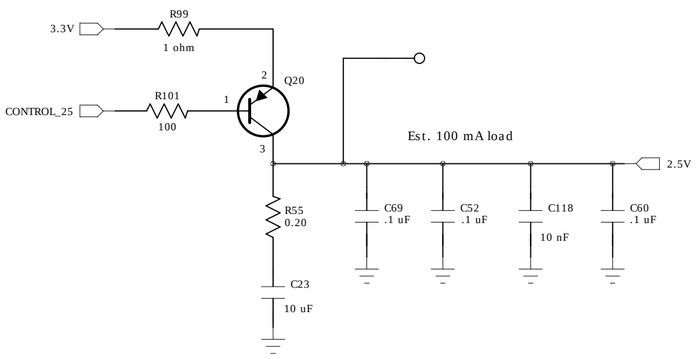
Ethernet Analog 3.3V



1.8V Regulator



2.5V Regulator

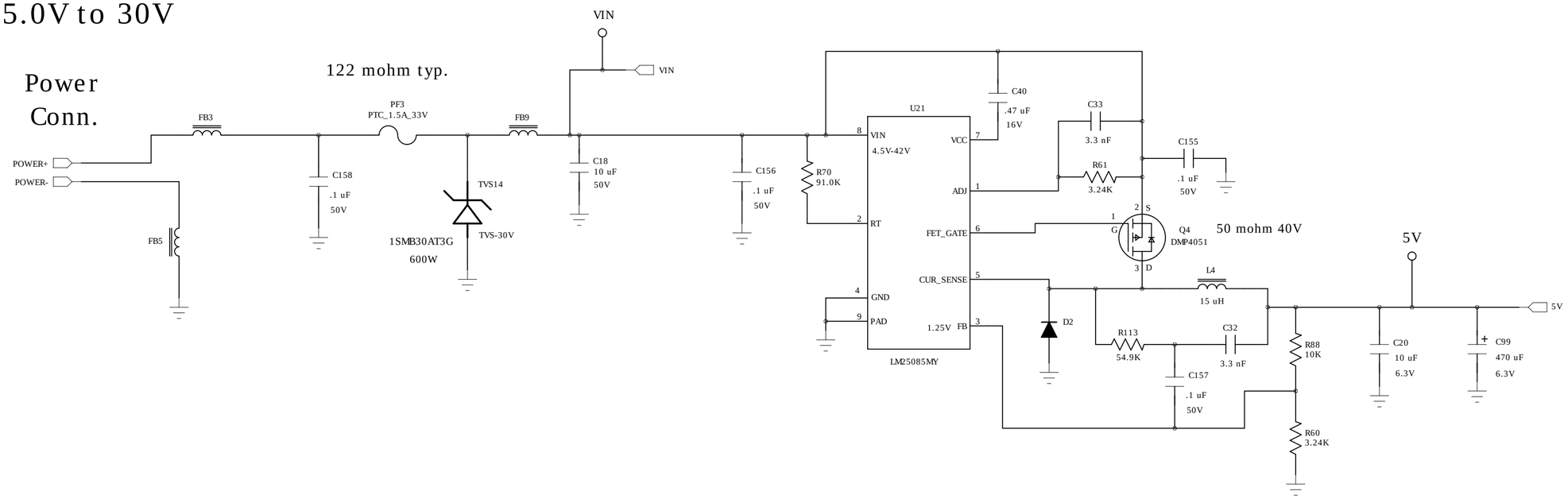


Technologic Systems		Date May 20, 2011
Title: TS-7558 Power Supplies		
Rev: A	Designer RLM	Sheet 4 of 12

5V Power Supply (2.0 Amps)

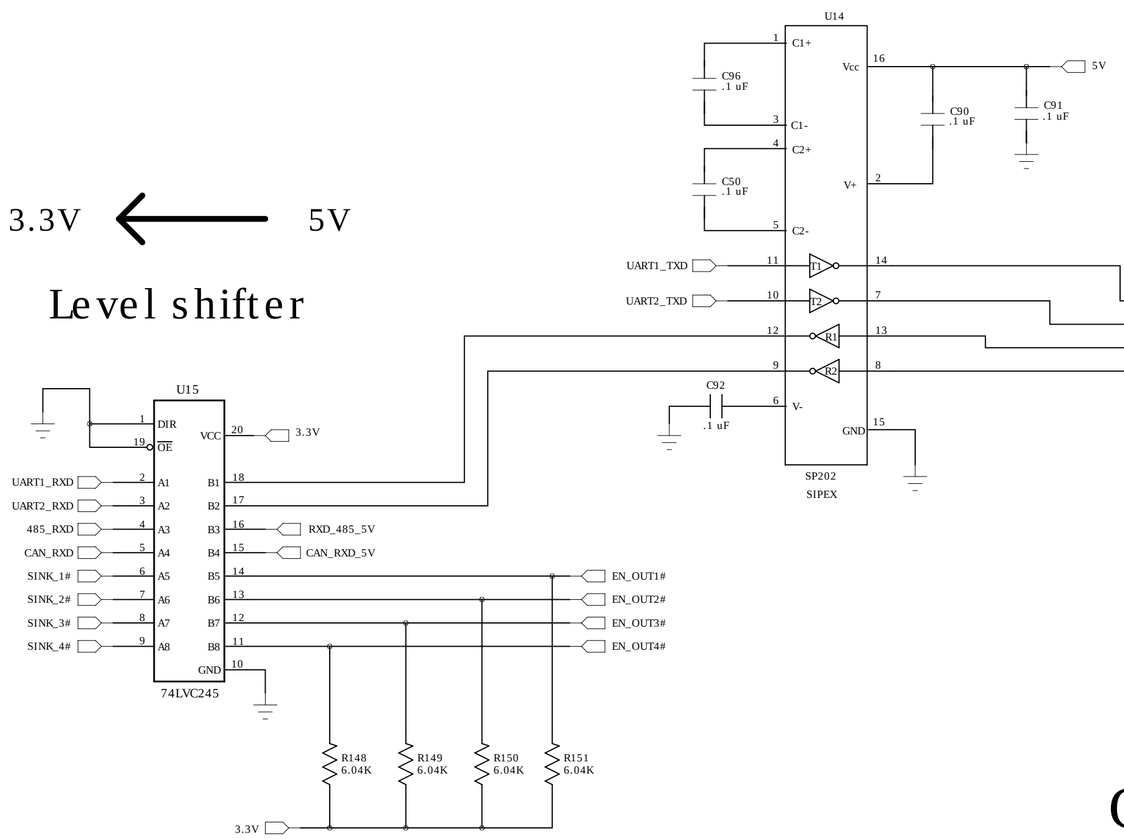
Input Power

5.0V to 30V

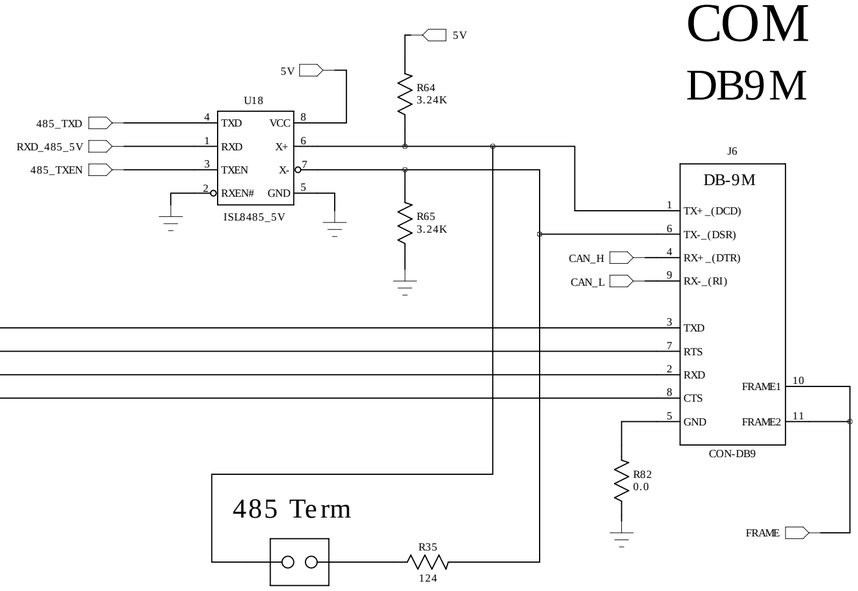


Technologic Systems		Date: May 20, 2011
Title: TS-7558 5V Power		
Rev: A	Designer	Sheet 5 of 12

RS-232 Transceiver

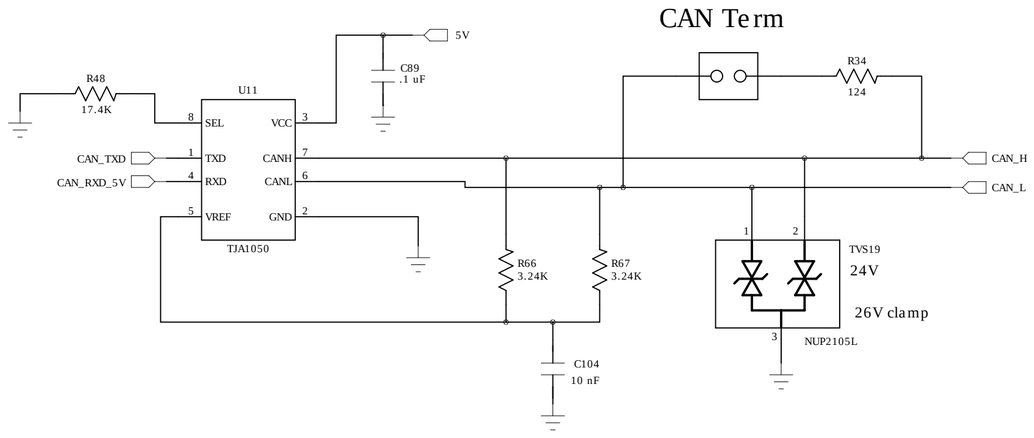


RS-485 Driver



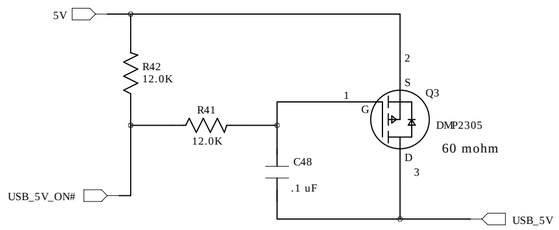
COM DB9M

CAN Tranceiver

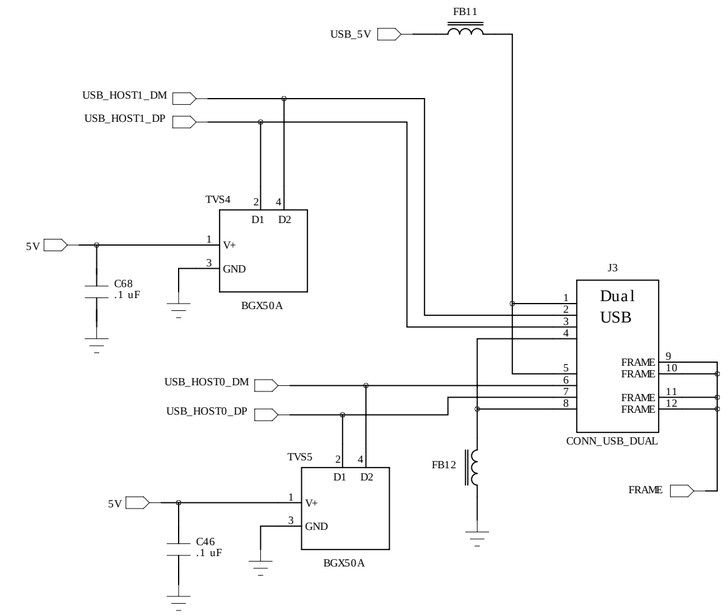


Technologic Systems	Date May 20, 2011	
Title: TS-7558 COM port, CAN, RS-485		
Rev: A	Designer RLM	Sheet 6 of 12

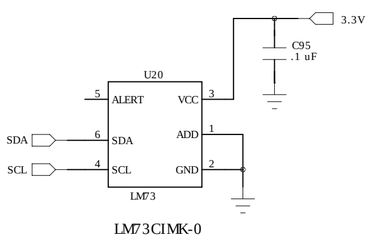
USB Power Switch



Dual USB Host

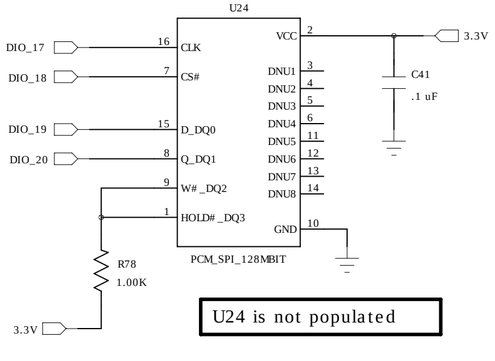


Temp Sensor



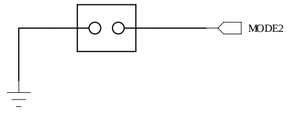
16 MB Phase

Change memory

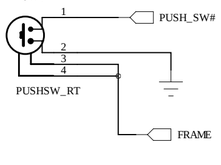


Force Boot to SD card

SD Boot



Push Switch

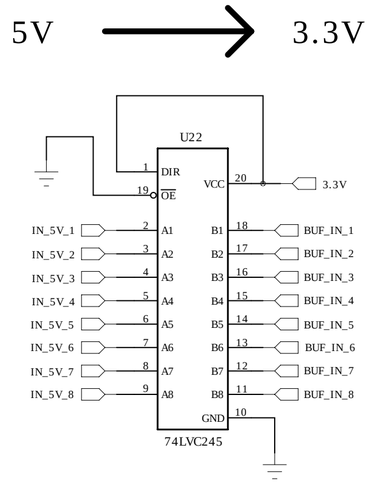


Technologic Systems		Date May 20, 2011
Title: TS-7558 USB, Temp Sensor		
Rev: A	Designer RLM	Sheet 7 of 12

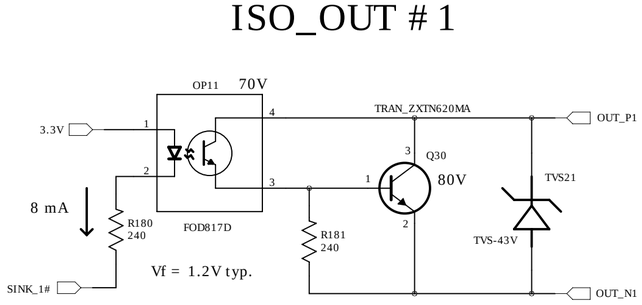
4 Isolated Outputs

Outputs rated for
200 mA at 40V max.

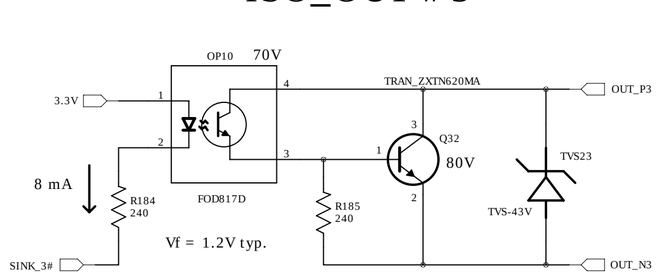
Buffer for Isolated Inputs



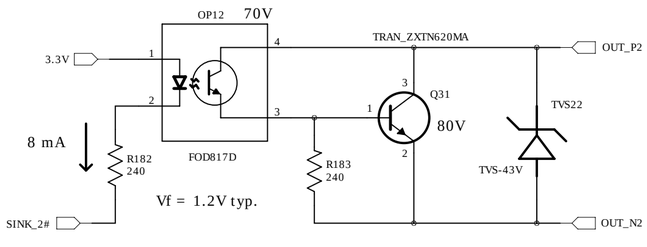
ISO_OUT # 1



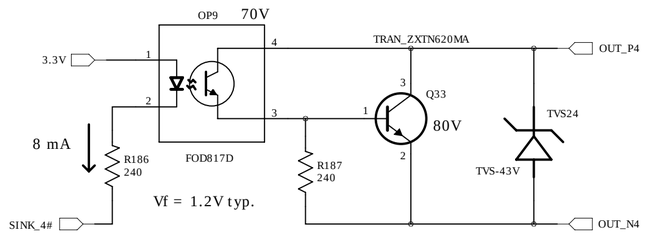
ISO_OUT # 3



ISO_OUT # 2



ISO_OUT # 4



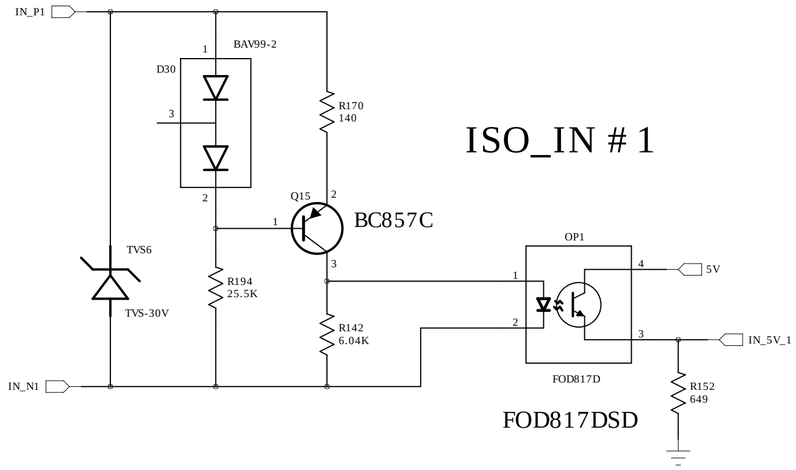
Technologic Systems	Date May 20, 2011	
Title: TS-7558 Isolated Digital Outputs		
Rev: A	Designer	Sheet 8 of 12

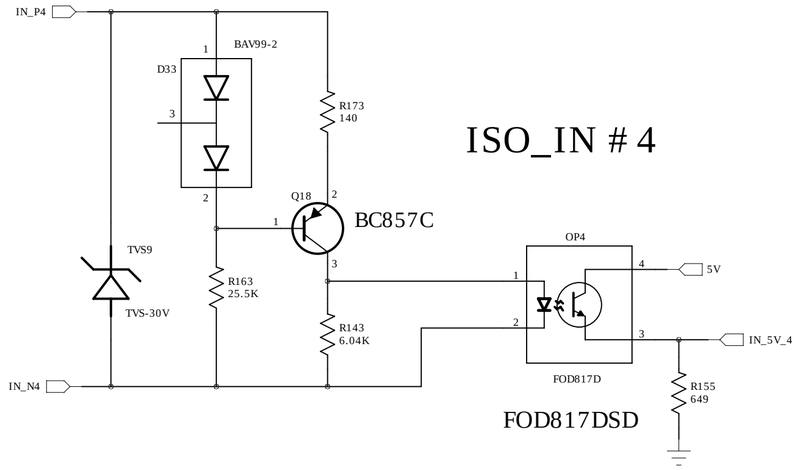
Isolated Inputs

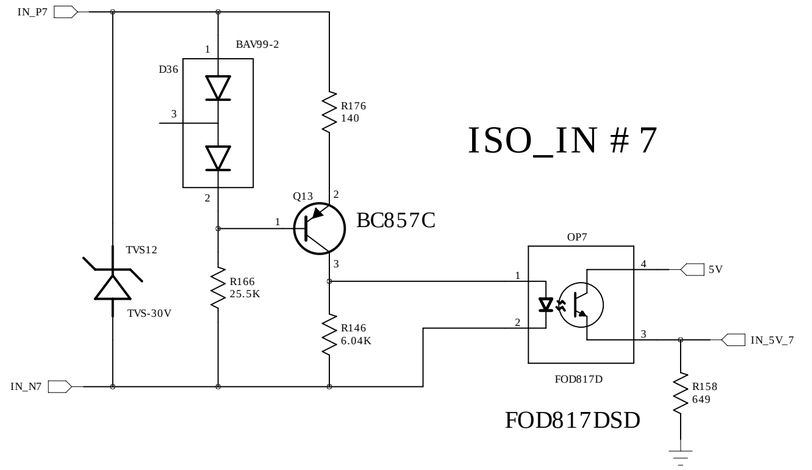
32V tolerant

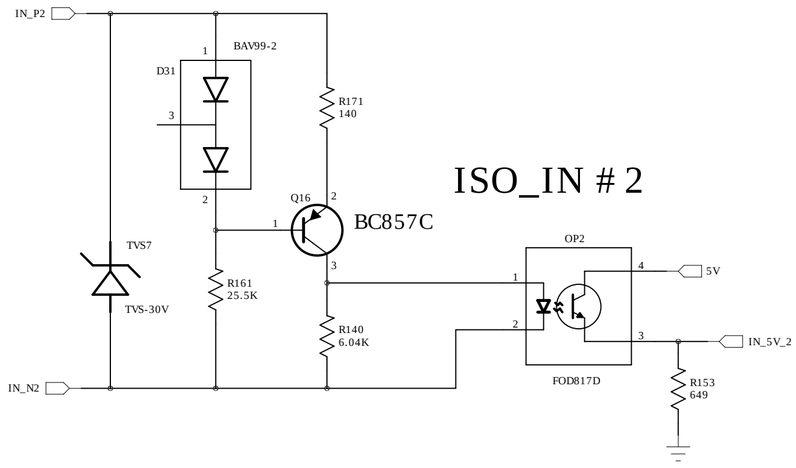
50 KHz Bandwidth

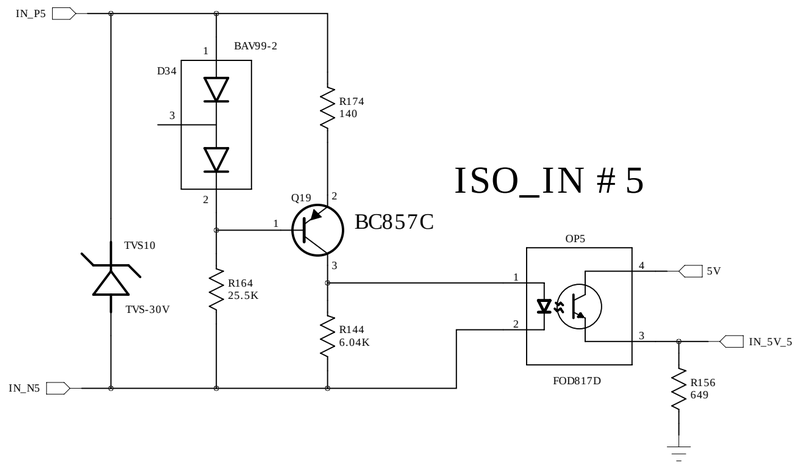
Logic high = 3V-30V

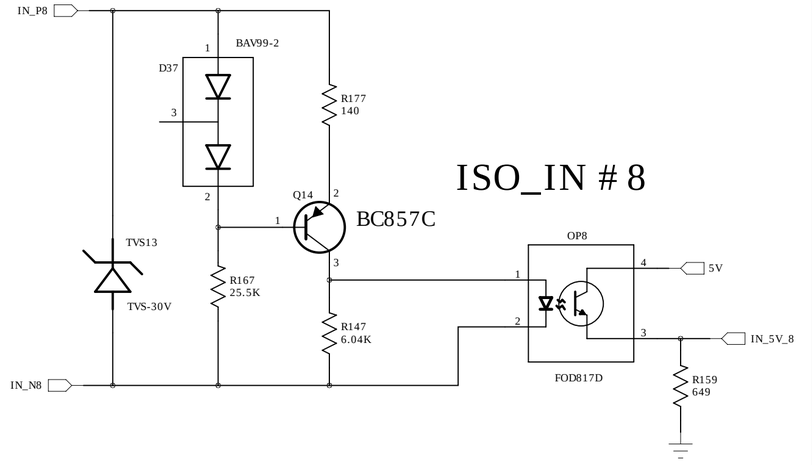


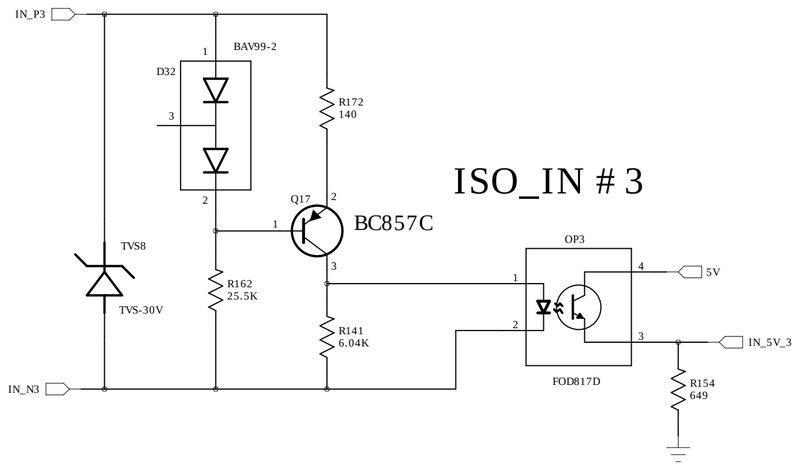


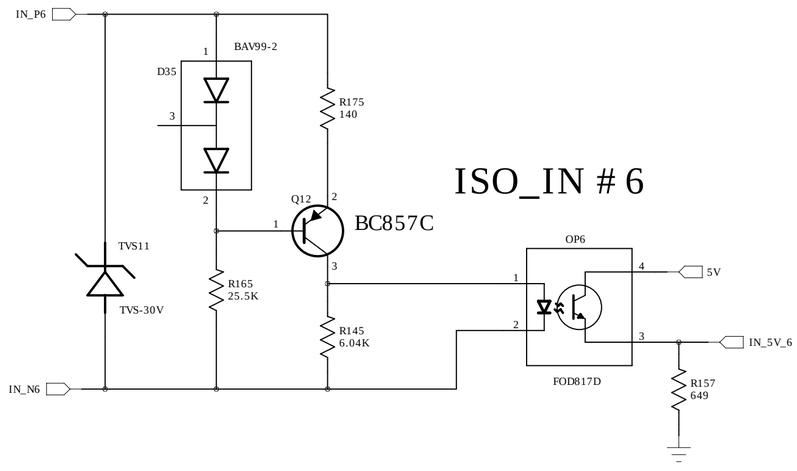












Technologic Systems		Date: May 20, 2011
Title: TS-7558 Isolated Digital Inputs		
Rev: A	Designer	Sheet 9 of 12

4 Channels of 12-bit A/D

ADC notes

Input Imedance = 70 Kohm

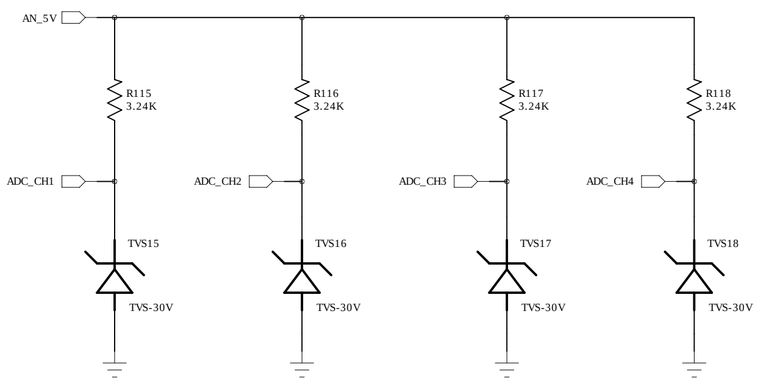
TVS adds 1000-3000 pF

typ. MUX ON resistance = 120 ohm

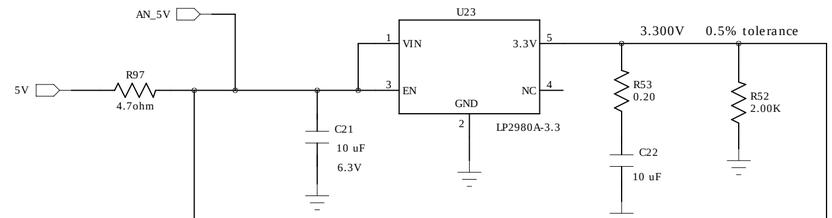
typ. Delta between chan = 10 ohm

Reading channel 0 allows calibrating out most error

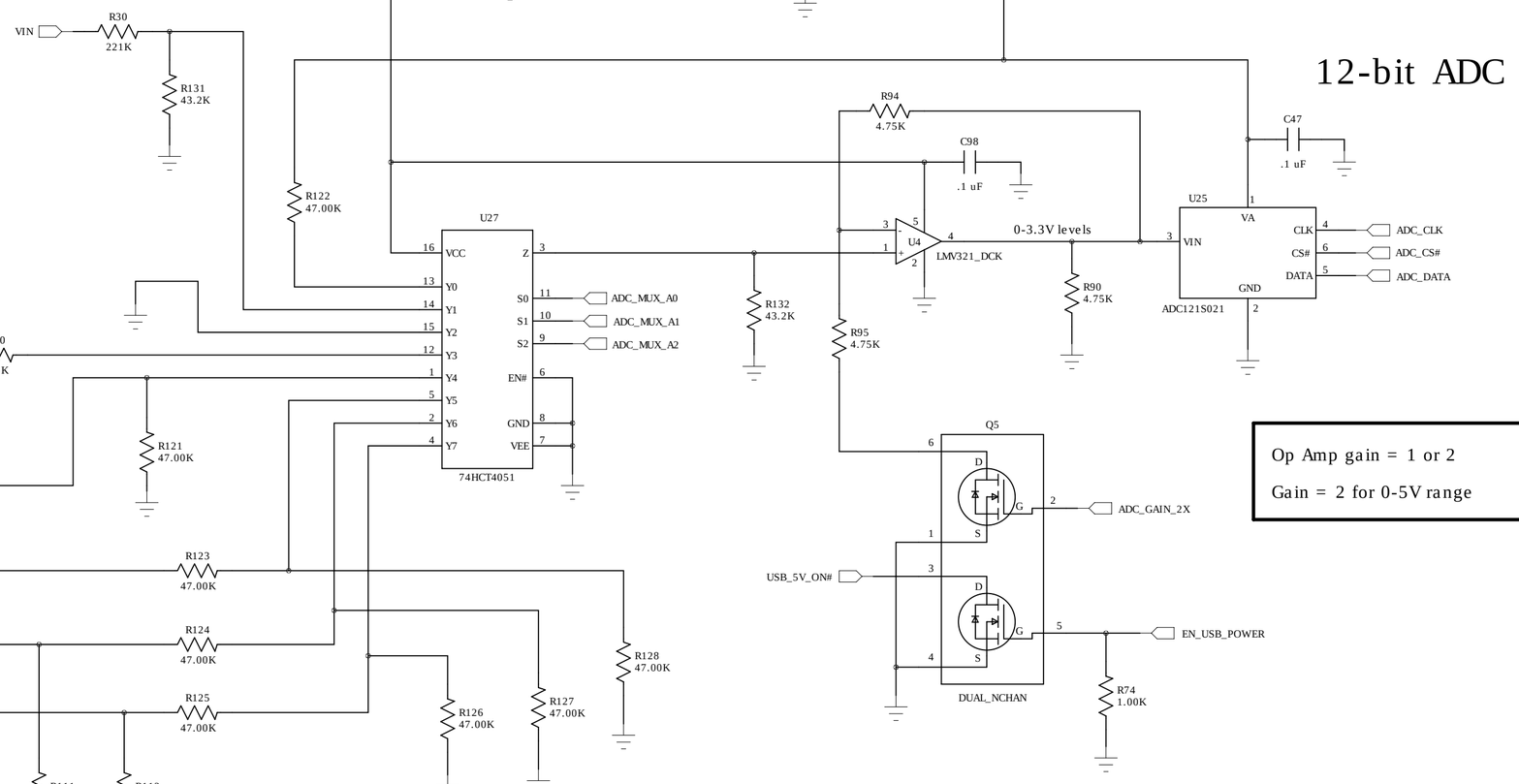
R115-R118 not normally Populated



Precision 3.3V Reg.



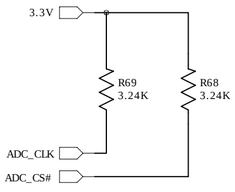
12-bit ADC



Op Amp gain = 1 or 2

Gain = 2 for 0-5V range

For I2C ADC

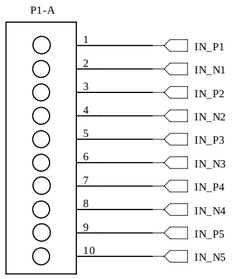


Technologic Systems		Date: May 20, 2011
Title: TS-7558 ADC		
Rev: A	Designer	Sheet 10 of 12

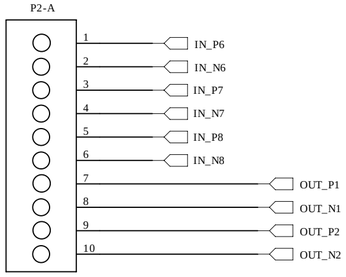
2x20 positions of Screw Terminals

Top Row

Left

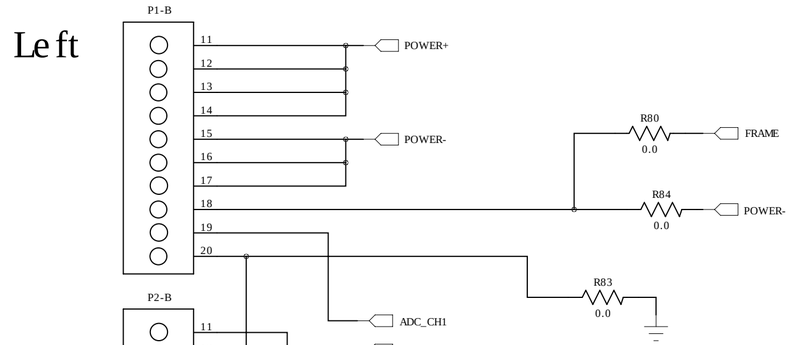


Right



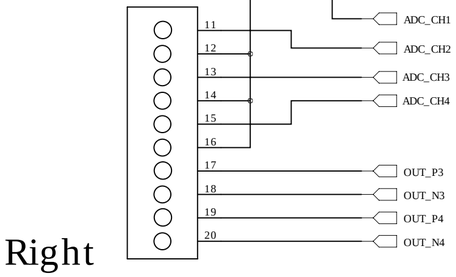
Bottom Row

Left



R80 is not populated

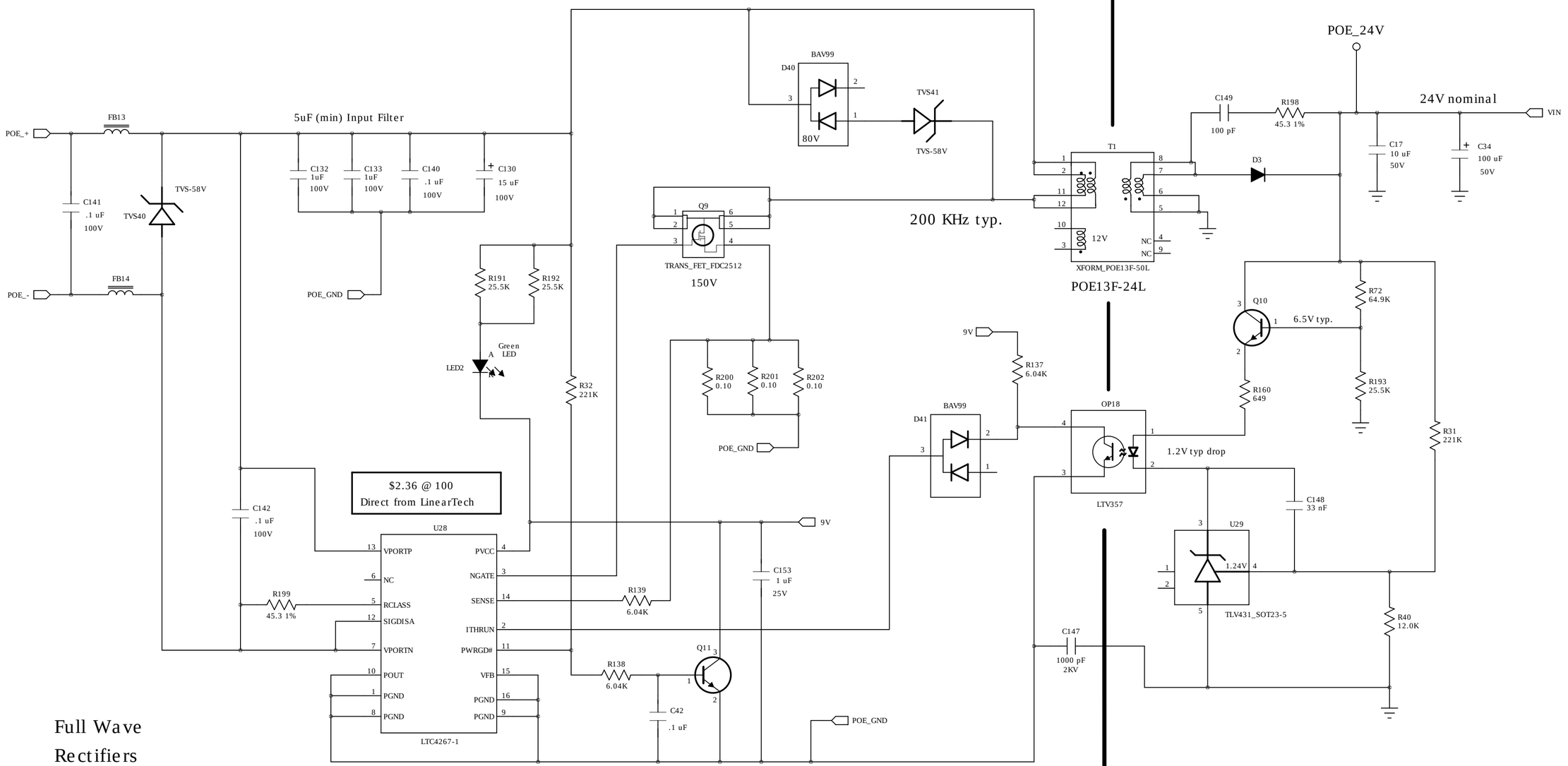
Right



Technologic Systems	Date May 20, 2011	
Title: TS-7558 Screw Terminals		
Rev: A	Designer	Sheet 11 of 12

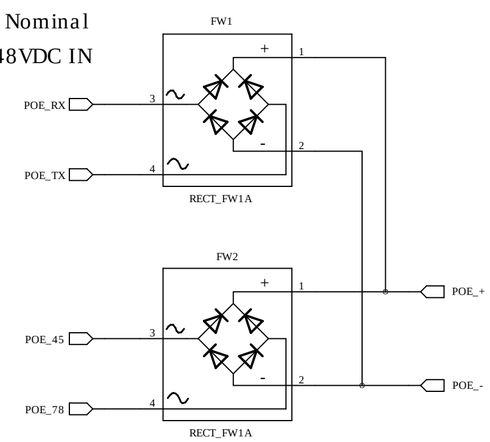
POE Side
48V DC Input

Isolated 24V Out



Full Wave Rectifiers

Nominal
48VDC IN



GND

Technologic Systems	Date May 20, 2011	
Title: TS-7558 POE		
Rev: A	Designer	Sheet 12 of 12